EF^2I: A new Bunch-by-Bunch Filling Pattern Measuring System at ELSA

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I hereby declare that this thesis was formulated by myself and that no sources or tools other than those cited were used.

Bonn, ...
Date Signature

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CHAPTER 1

Introduction

1.1 Motivation

In the project reported in this thesis a fast readout system for a Beam Position Monitor (or short BPM) in the Stretcher ring of the electron accelerator ELSA, called EF^{2}I[1], has been developed. With this system, the transversal position and the charge of each single electron bunch in the beam can be resolved.

At ELSA, electrons are accelerated within three consecutive acceleration stages. The new readout system is operated in the Stretcher ring, which is the last stage. Here, the electron beam position is measured with a BPM. A BPM consists of four electrically isolated electrodes, which are arranged in the beam pipe around the beam. The electrons pass through the BPM, therefore a measurable electric signal is induced onto the electrodes. This non destructive measurement can be performed parasitically while the accelerator provides the electron beam for the experiments. The induced signal contains information about the beam position, but also about the overall charge of each bunch in the beam.

For beam position measurements in the Stretcher ring, the analog signals of the four BPM channels are processed further, before they are digitized. Until now, this processing involves averaging over 2000 revolutions of all 274 bunches due to hardware constraints, allowing to extract only transversal information about the beam as a whole. The new readout system developed in this thesis uses a novel broadband preprocessing of the signals and a faster readout, providing position information not only about the whole beam, but for every individual bunch, also enabling a measurement of their charges. The sequence of bunch charges is also called the filling pattern of the beam, as it indicates "how full" the individual buckets are.

By measuring the position with single bunch resolution, the tune can be determined in the vertical and horizontal plane by excitation of one bunch in the beam, which is possible with the bunch-by-bunch feedback system. The measurement of the filling pattern can be used to adapt and improve the basic injection from the Booster synchrotron to the Stretcher ring to the individual needs. Furthermore, the accumulation of ions can be reduced by specific gaps in the filling pattern ([1]). These gaps can be created by the bunch-by-bunch feedback system and verified by the EF^{2}I system.

[1] short for **E**LSA **F**ast **F**illingpattern **I**maging

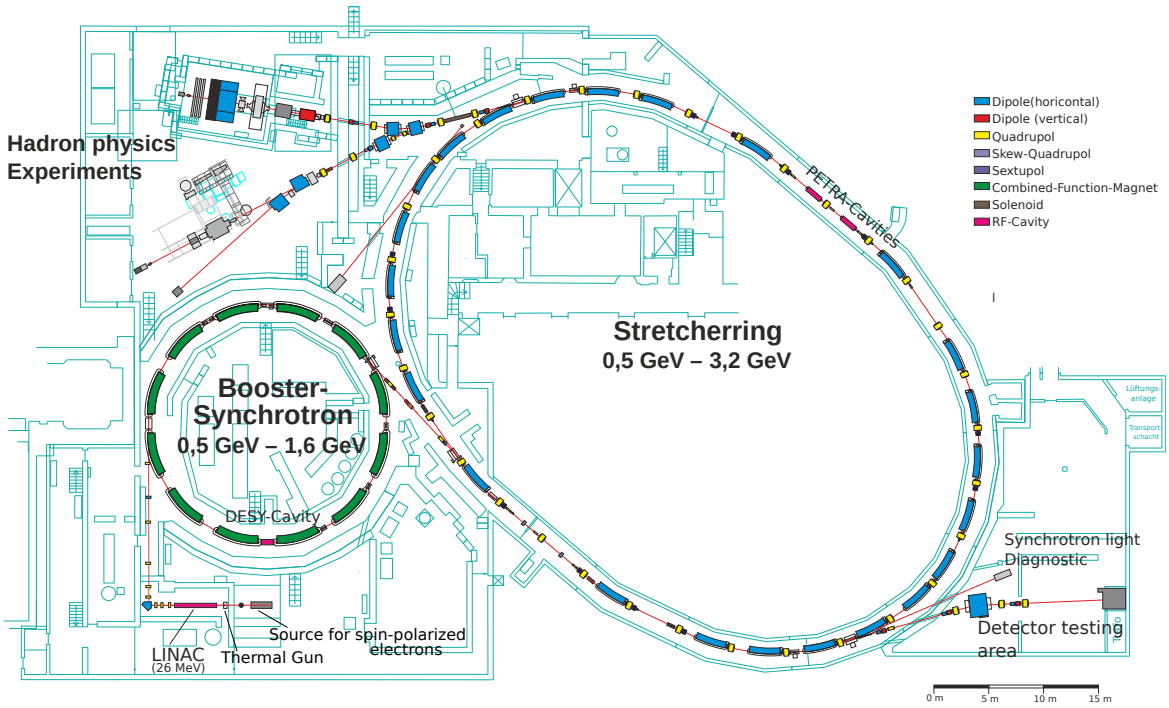


Figure 1.1: Overview map of the accelerator facility in the basement of the physics institute.

1.2 History of Electron Accelerators at the University of Bonn

In 1953 the decision was made to build an electron accelerator at the Institute for Physics at the University of Bonn, leading to the first electron synchrotron with strong focussing in Europe, which was brought into operation in 1958. It was built under the advice of Wolfgang Paul and achieved a maximum beam energy of 500 MeV. The synchrotron was replaced by a larger accelerator in 1967, which accelerated the beam up to an energy of 2.5 GeV. This so called Booster synchrotron was rededicated as a pre-accelerator with lower beam energy in 1987, when the new Stretcher ring ELSA (**EL**ektronen **S**tretcher **A**nlage[2]) was completed, allowing for a maximum beam energy of 3.2 GeV.

1.3 Present Accelerator Facility

Figure 1.1 shows an overview map of the facility in the basement of the Institute for Physics. An electron beam is generated and pre-accelerated to a kinetic energy of about 50 keV utilizing either a thermal gun or a source for spin-polarized electrons. The electrons are then accelerated in the linear accelerator (LINAC) up to a total energy of 26 MeV. For the next acceleration step, the electrons are injected into the Booster synchrotron, which has a circumference of 69.9 m, so that the relativistic electrons have a revolution time of 232 ns. During the acceleration process, the magnetic field, which bends the electrons onto their orbit, increases until the extraction energy is reached. This ramping of the magnetic fields is synchronized with the electric supply mains (50 Hz), resulting in an acceleration

[2] (English: Electron Stretcher Facility, the Stretcher ring is the namesake for the whole facility)

from 26 MeV to the extraction energy of 1.2 GeV in less than 10 ms and a new filling every 20 ms. Subsequently, the electrons are injected into the Stretcher ring, the largest synchrotron of the facility.

In the Stretcher ring, the electron beam with a current of typically approximately 30 mA can be accelerated to energies between 0.5 GeV and 3.2 GeV. The revolution time of the beam in the 164.4 m long ring is 548 ns. In the two circular accelerators, the electrons are accelerated with a standing wave with a frequency of 499.67 MHz in the cavities. This method of acceleration leads to a microscopic beam structure of electron bunches, with a bunch length in the order of 100 ps at a time interval of 2 ns .

The electron beam can be extracted to one of two hadron physics experiments, CB-ELSA[3] and BGO-OD[4], or to the detector testing area, including a synchrotron light diagnostic site with a streak camera.

These and further information about the accelerator facility can be found in [4], [5] and [6].

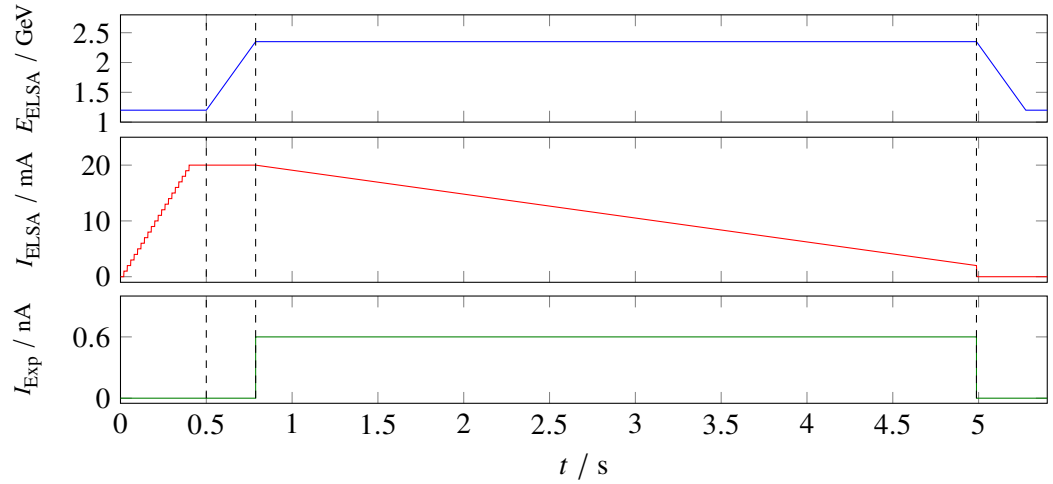
1.4 Modes of Acceleration

The accelerator operates in three modes, which are illustrated in figure 1.2. The Booster Mode is selected for the experiments, which require a continuously extracted electron beam, but a different mode can also be used for diagnostic purposes. The three available modes are briefly described below:

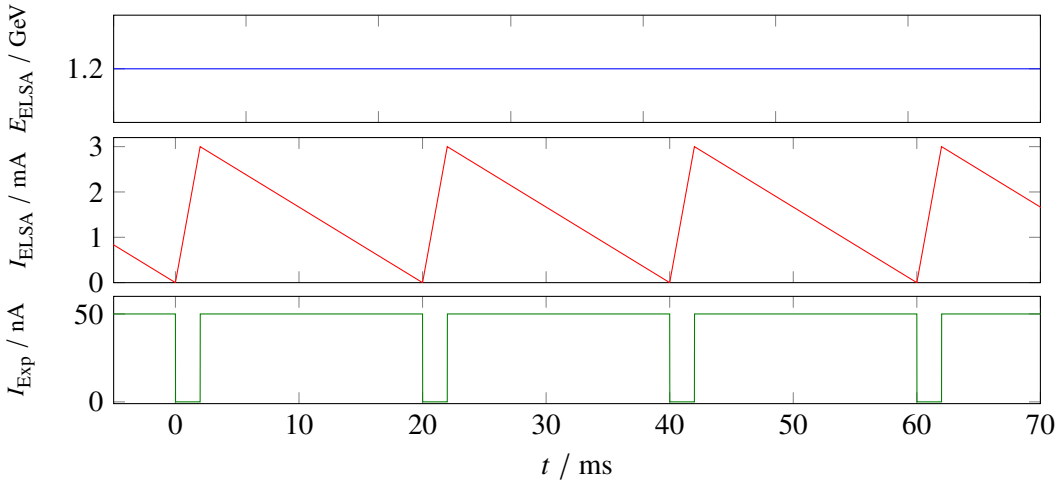
- Booster Mode: The Stretcher ring is filled with injections from the Booster synchrotron, until a desired beam current is injected, which is typically reached with 21 injections. The electrons are accelerated to a set beam energy and are extracted to the experiments. A cycle typically lasts about 6 s, from which the injection takes less than 0.5 s and the extraction about 4.5 s.
- Stretcher Mode: A single filling of the Booster synchrotron is injected into ELSA and is extracted without further acceleration until a new injection starts after 20 ms. With this, the extraction time of 232 ns from one Booster synchrotron filling to ELSA is stretched to almost 20 ms for extraction to the experiments. This mode is currently not available.
- Syli Mode: Several electron injections from the Booster synchrotron are accumulated in the Stretcher ring until a desired beam current of typically around 30 mA is reached. The electrons are accelerated to the set beam energy and then are stored for a certain time span ranging in the order of minutes to hours.

[3] short for *Crystal Barrel*. For more information see [2]

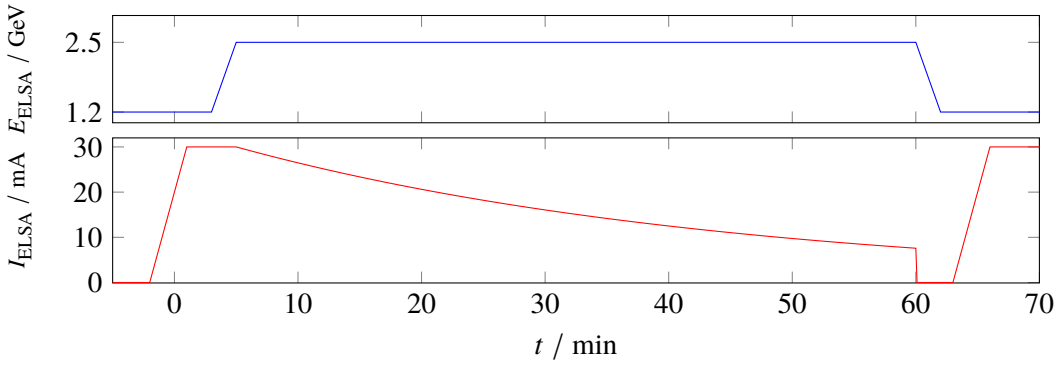
[4] short for *Bismuth Germanium Oxide - open dipole*. For more information see [3]



(a) Booster Mode



(b) Stretcher Mode



(c) Syli Mode

Figure 1.2: Schematic depiction of current I_{ELSA}, total energy E_{ELSA} of the accelerated electrons in ELSA (what is written here only for the stretcher ring) and extracted current I_{Exp} to the experiment with typical values at ELSA [7].

CHAPTER 2

Background Information

This chapter first introduces some basic principles about physics in circular accelerators[1]. Then the BPM is presented as a diagnostic system for the electron beam. This is followed by a part in which the basics of an FPGA and an ADC as essential electronic components of this work are given.

2.1 Beam Dynamics

In an electron synchrotron, which is a circular accelerator, the electrons are deflected onto a circular path, the so called orbit, with the help of magnetic guiding fields. In these fields $\vec{B}$, a Lorentz force

$$\vec{F}_{\mathrm{L}} = q(\vec{v} \times \vec{B}) \tag{2.1}$$

exerts on the electrons with charge q and velocity $\vec{v}$. The main magnetic fields can be distinguished between dipole and quadrupole fields. The magnetic field lines in dipole magnets are perpendicular to the deflection radius and the direction of motion of the electrons and are responsible for bending the electrons onto a circular path. Quadrupole fields, which each have a component horizontal and vertical to the direction of electron movement, are used to focus the beam.

To describe a particle in the accelerator, a co-moving coordinate system is used, as shown in figure 2.1. The origin of the coordinate system moves with an imaginary particle on the design orbit,

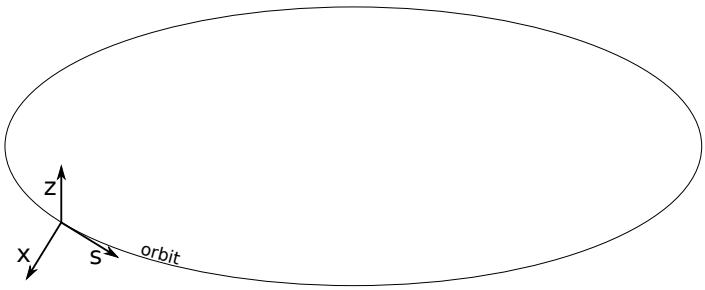


Figure 2.1: In a particle accelerator typically a co-moving coordinate system is used. The axis s always points in the direction of the design orbit, x is in the horizontal plane and z in the vertical.

[1] Descriptions in this chapter predominantly based on the book [8]

where the s axis always points in the direction of movement of the particle. x and z axis point in the horizontal and in the vertical direction, respectively. A longitudinal Δs, a horizontal Δx and a vertical Δy displacement describe the trajectory of an individual particle in relation to the design orbit.

2.1.1 Longitudinal Beam Dynamics

In an electron synchrotron, the electrons are accelerated in acceleration cavities by an electric field, sinusidial oscillating in time with a fixed high frequency ν_{acc} and a maximum voltage amplitude U_0. From this, it follows that the electron beam has not a continuous, but a bunched structure. The effective acceleration voltage U_{ref} for a revolution depends on the effective acceleration phase $\Psi_0 + \Delta\Psi$, where Ψ_0 is the acceleration phase of the beam and $\Delta\Psi$ the deviation of the individual particles phase. The absolute energy gain per revolution E_{rev} is given by

$$E_{\mathrm{rev}} = \mathrm{e}U_0 \sin\left(\Psi_0 + \Delta\Psi\right) - W_{\mathrm{rev}} \tag{2.2}$$

with the electron charge e and the loss of energy per turn W_{rev} due to synchrotron radiation, which is given by [8, chapter6]

$$\Delta W_{\mathrm{rev}} = \frac{\mathrm{e}^2\beta^3}{3\epsilon_0\left(m_{\mathrm{e}}c^2\right)^4}\frac{E^4}{R} \tag{2.3}$$

with the electron mass m_{e} and the bending radius R. If the electrons are not further accelerated or decelerated, the energetic equilibrium

$$\mathrm{e}U_0 \sin\left(\Psi_0\right) = W_{\mathrm{rev}} \tag{2.4}$$

holds. Here, the ideal acceleration phase Ψ_0 is fixed by the synchrotron radiation losses of the beam. The effective acceleration phase depends on the point in time, at which the individual electron arrives at the acceleration cavity. Figure 2.2 shows the principle of phase focusing, which ensures that the phase differences of the individual particles to Ψ_0 do not increase over time. It is based on the fact that the relative momentum deviation $\Delta p/p_0$ of a relativistic electron is related to the relative change of the path length $\Delta L/L_0$ which is given by

$$\frac{\Delta L}{L_0} = \alpha_{\mathrm{c}}\frac{\Delta p}{p_0}. \tag{2.5}$$

Here, p_0 is the momentum of a particle on the design orbit and L_0 is the length of this orbit. Δp and ΔL are the respective deviations of a real particle and α_{c} is the momentum compaction factor. For the electrons in the beam, three cases for the momentum deviation occur

$$\frac{\Delta p}{p_0} < 0, \qquad \frac{\Delta p}{p_0} = 0 \quad \text{and} \quad \frac{\Delta p}{p_0} > 0. \tag{2.6}$$

Due to the shortening of the path length for electrons with negative Δp as they are deflected by dipoles to a narrower orbit, these electrons arrive earlier at the acceleration cavity, than electrons on the ideal orbit. The extension of the path length for electrons with positive Δp as they are deflected by the dipoles onto a wider orbit, resulting in a delayed arrival in the acceleration cavities. In figure 2.2, the effective acceleration voltage is shown for $\Delta p/p_0 < 0$ in red, $\Delta p/p_0 = 0$ in green and $\Delta p/p_0 > 0$ in

yellow. The different energy gains in combination with the path length variation mentioned above lead

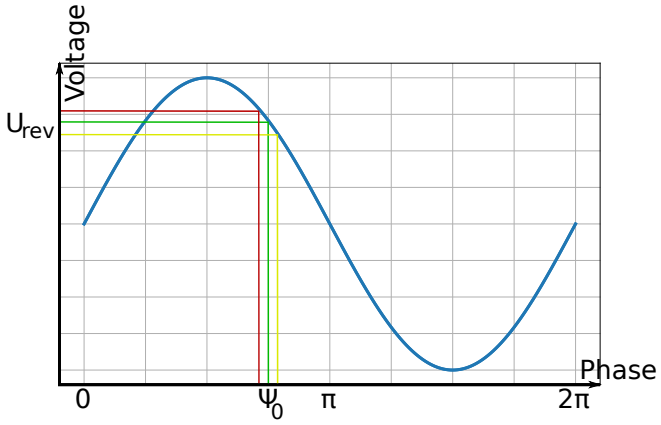


Figure 2.2: In this plot the acceleration field in the cavities in reference to the acceleration phase is shown. A particle on the design orbit is accelerated at phase Ψ_0. A particle arriving earlier in the acceleration cavity, will be accelerated at the phase marked in red. A particle arriving later will be accelerated at the phase marked in yellow.

to a longitudinal oscillation of the electrons with the so called synchrotron frequency ν_s around the energy E_0 of a particle on the design orbit. The equation of motion for small deviations of E can be written as [8, chapter 6]

$$\Delta\ddot{E} + 2\alpha_s\Delta\dot{E} + (2\pi\nu_s)^2\Delta E = 0 \tag{2.7}$$

with a longitudinal damping constant α_s and the synchrotron frequency given by [8, (compare to chapter 5.6)]

$$\nu_s = \nu_\mathrm{rev}\sqrt{-\frac{eU_0 n\cos\left(\Psi_0\right)}{2\pi\beta^2 E}\left(\alpha_\mathrm{c} - \frac{1}{\gamma^2}\right)}. \tag{2.8}$$

For phase-correct acceleration of the bunches with fixed $\Psi_0$in the cavities, the acceleration frequency ν_acc and revolution frequency ν_rev have to equal a harmonic number $n \in \mathbb{N}$, which also indicates the number of buckets in the accelerator.

The longitudinal oscillation can be characterized by the longitudinal tune Q_s, which can be determined by

$$Q_\mathrm{s} = \frac{\nu_s}{\nu_\mathrm{rev}}. \tag{2.9}$$

2.1.2 Transversal Beam Dynamics

In the transversal plane, the electron's trajectory is described by differential equations of Hillian type [8, compare to chapter 3]

$$x''(s) = \left(\frac{1}{R^2(s)} - k(s)\right)x(s) = \frac{1}{R(s)}\frac{\Delta p}{p_0} \quad \text{and} \quad z''(s) + k(s)z(s) = 0 \tag{2.10}$$

in the horizontal and vertical plane, with deflection radius $R(s)$ of an electron in a dipole and quadrupole strength $k(s)$. Here, only deflection by dipoles in horizontal direction is assumed. The solution trajectories ($x(s)$ and $z(s)$) to these equations are equal to those of a pseudo-harmonic oscillator. Here, the electrons perform quasi-sinusoidal oscillations in the horizontal and vertical plane, which are called betatron oscillations. The horizontal and vertical tunes are given by the number of betatron oscillations per revolution.

Due to so called optical resonances in the accelerator in which the electron trajectories with certain transversal tunes are destabilized due to magnetic errors, it can not be chosen arbitrarily (for more information see [8, chapter 3]).

2.1.3 Beam Structure

In both, the Booster synchrotron and in the Stretcher ring, an rf-field with a frequency ν_{acc} of 499.67 MHz is used to accelerate the electron beam. In the Stretcher ring, the microscopic[2] beam structure is given by the acceleration process itself, resulting in bunches with a distance of 2 ns, while the macroscopic[3] beam structure is mainly caused by the injection from the Booster synchrotron and can be altered by shifting the injection time (for more information on the timing of the injection, see [9, chapter 6.5]).

The longitudinal bunch length σ_s is given by (compare to [10, chapter 5.4])

$$\sigma_s = \frac{\alpha_s \beta c}{2\pi \nu_s} \left(\frac{\Delta E}{E} \right)_{\mathrm{Sync}} . \tag{2.11}$$

Where $\left(\frac{\Delta E}{E}\right)_{\mathrm{Sync}}$ is the energy uncertainty given by synchrotron oscillation. An electron which has the ideal energy, i.e. is accelerated with the acceleration phase of the beam Ψ_0 in the cavity, can lose energy by emitting a synchrotron radiation photon, causing it to deviate from the target phase and oscillate around it. Leading to a linear proportionality of σ_s to E, if ν_s and α_s kept constant.

In a bunch, which in first order has a GAUSSIAN shaped charge distribution, the longitudinal bunch current I_b can be expressed as

$$I_{\mathrm{b}}(t) = \frac{\beta c q_{\mathrm{b}}}{\sqrt{2\pi}\sigma_{\mathrm{s}}} \exp\left(\frac{-t^2 \beta^2 c^2}{2\sigma_{\mathrm{s}}^2} \right) \tag{2.12}$$

with the charge of the bunch q_{b}, the bunch length σ_{s}[4], the bunch velocity βc and the time t. The line charge density of the bunch is given by

$$q_{\mathrm{b}}(t) = \frac{I_{\mathrm{b}}(t)}{\beta c}. \tag{2.13}$$

The electron beam is considered to be centred in a round beam pipe. Due to electric inductance, the electrons will induce an opposite charge onto the conducting beam pipe, which can be utilized for

[2] Buckets with a distance of 2 ns in the beam, which can be filled with electrons and than are called bunches.

[3] The contiguous filling pattern of the beam.

[4] Care has to be taken, as often the length of the bunch corresponds to the full width half maximum (FWHM). The relationship between the two quantities is given by $\mathrm{FWHM} = 2\sqrt{2 \cdot \ln(2)} \cdot \sigma_{\mathrm{s}}$.

diagnostic purposes as will be discussed in the next section.

2.2 Beam Diagnostics

To optimize the acceleration process in a particle accelerator, it is important to characterize the beam. This can be done with destructive measurements like a beam screen[5], which normally is not used in circular accelerators, because the beam is lost due to the measurement, or with non destructive systems like a beam position monitor (BPM) or a synchrotron light camera[6]. In the following the functional principle of a BPM is elaborated in more detail.

2.2.1 Beam Position Monitors

With a BPM the horizontal and vertical beam position can be measured. While different kinds of BPMs are available, in the following the focus is on BPMs with four button pick-up electrodes, which couple to the electric field of the electron beam.

In ELSA two essentially different kinds of BPMs with button pick-up electrodes are installed: one type was designed at DESY[7] the other at ESRF[8]. They have different geometries, but basically work in the same way. The fundamental arrangement of the four electrodes around the beam pipe can be seen in figure 2.3.

The electrodes of the BPMs couple to the electromagnetic field of the bunches. For ultra-relativistic electrons, the resulting electric field lines can be considered to be purely transversal in first order, such that the induced current onto the beam pipe with infinite conductivity is given by $-I_\mathrm{b}(t)$. Furthermore, the induced current density on the wall perpendicular to the direction of motion of the electrons, depends on the geometry of the beam pipe and on the beam position. So the charge induced to a perfectly conducting electrode by one bunch with a line charge density corresponding to equation 2.13 is proportional to

$$q_\mathrm{e}(t) \propto -q_\mathrm{b}(t) = -\frac{I_\mathrm{b}(t)}{\beta c}. \tag{2.14}$$

The proportionality contains time-independent factors such as the geometry of the electrode and the position of the bunches.

Because of the capacitive coupling of the electrodes, the measured current flowing onto the capacitance is proportional to the time derivative of $q_\mathrm{e}(t)$ and can be expressed as

$$I_\mathrm{e}(t) \propto -\frac{\mathrm{d}I_\mathrm{b}(t)}{\mathrm{d}t}\frac{1}{\beta c} \propto -\frac{q_\mathrm{b}\beta^3 c^3 \cdot t}{\sqrt{2\pi}\sigma_\mathrm{s}^3 \beta c} \exp\left(\frac{-t^2\beta^2 c^2}{2\sigma_\mathrm{s}^2}\right). \tag{2.15}$$

As the measurement of the induced signal by the bunches is performed over a $50\,\Omega$ termination resistor, the measured signal is a voltage V_e, which is given by $50\,\Omega \cdot I_\mathrm{e}(t)$. It can be shown that the signal

[5] A Fluorescence screen, on which the beam position and the beam shape can be visualized.

[6] Due to synchrotron radiation, the electrons emit photons mostly in forward direction. These can be imaged to deduce the transversal beam profile. With a streak camera it is also possible to gain time information about the beam. For more information see [11, chapter 3.2]

[7] **D**eutsches **E**lektronen **Sy**nchrotron in Hamburg, Germany

[8] **E**uropean **S**ynchrotron **R**adiation **F**acility in Grenoble, France

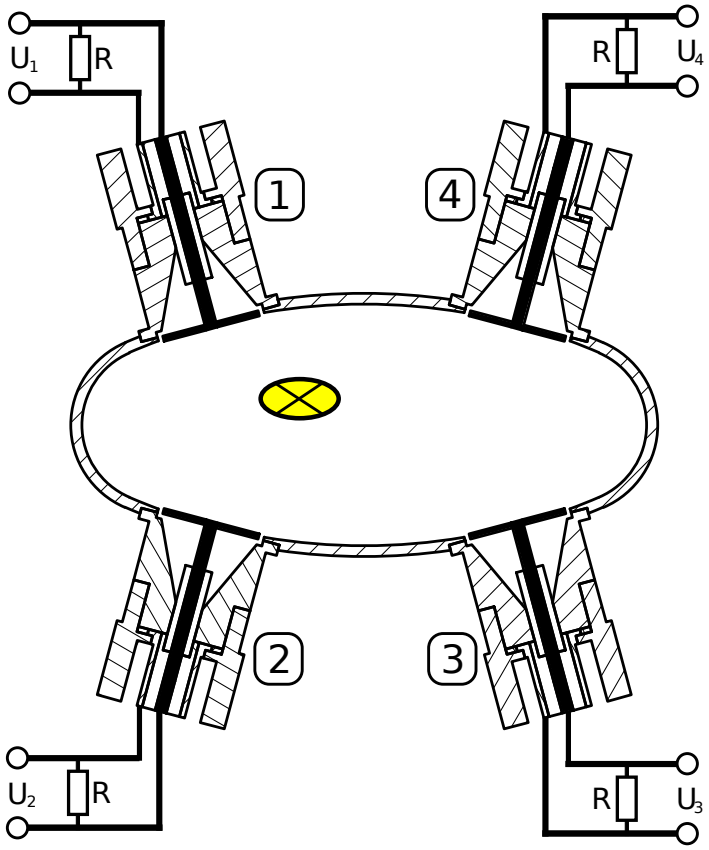


Figure 2.3: Schematic drawing of a BPM with button pick-up electrodes. The electrodes are electrically isolated and are arranged around the centre of the beam pipe. Due to synchrotron radiation being emitted in electron accelerators mainly in the horizontal plane, positioning of the electrodes in this plane is avoided. An electron beam propagating into the image plane is shown in yellow. Beam size is not to scale.

peaks occur at $t = \pm\sigma$. The bunch length varies with beam energy, the momentum compaction factor and the synchrotron frequency (see 2.11). Accordingly, the peak does not have the same position in time for different bunch lengths. The amplitude of the peaks is proportional to

$$V_{\mathrm{e,\,max}} \propto \pm\frac{q_\mathrm{b}}{\sigma_\mathrm{s}^2}. \tag{2.16}$$

A realistic BPM will have different kinds of attenuations for example from the cables, which all are dependent on the signals frequency, but not on its amplitude.

Position measurement

As the induced current density onto the four electrodes depends on the beam position, it can be used to measure the position of the passing electron beam. In [12, chapter 6] it is described, that the beam position can be determined from the BPM signals, by calculating the differences between the signals in the horizontal and vertical planes and dividing them by their sum. In an analog signal processing the 499.667 MHz basic signal is mixed with a 489 MHz signal. With a narrow-band-pass filter the

10.7 MHz component of the mixed signal is selected for digitization, whereas all other components are filtered out. Subsequently, the signal is digitized and the quotient proportional to the position in horizontal and vertical plane can be calculated as

$$q_x := \frac{\Delta_x}{\Sigma} = \frac{(U_1 + U_2) - (U_3 + U_4)}{U_1 + U_2 + U_3 + U_4} \tag{2.17}$$

$$q_y := \frac{\Delta_y}{\Sigma} = \frac{(U_1 + U_4) - (U_2 + U_3)}{U_1 + U_2 + U_3 + U_4} \tag{2.18}$$

with U_i being the voltage measured at the electrode i, see figure 2.3. For both planes the positions with their corresponding pair of quotients must be measured once and stored in a calibration map. Then the calculated quotients can be compared with this calibration map and conclusions can be drawn about the position of the beam. This calculation is not only valid for the whole beam, but also for single bunches.

Bunch by Bunch Feedback System

The bunch by bunch feedback system from Dimtel Inc. is used to damp emerging coherent beam oscillations. To do so, a BPM is read out and a correction signal is calculated for each bunch and is applied for the individual bunches via a broadband kicker. In addition, the system can be used to measure longitudinal, horizontal and transversal tunes of the beam and excite specific bunches.

2.3 Analog to Digital Converter

With an ADC[9] it is possible to convert an analogue signal into a digital signal, which can be further processed or stored by an FPGA (see 2.4). The input signal can be continuous in time and amplitude, the digital output signal is a quantized signal with discrete amplitudes at discrete points in time. Beside the signal to be sampled, the ADC also needs to get a clocking signal, which defines the point in time of the sampling (sampling time). Of course the digital signal is not directly present at the output pins, when the input signal is present. This delay is called *data latency* and, depending on the ADC type, can be greater than the clocking frequency, since the data can be digitized with several successive stages inside the ADC. Therefore the *data latency* is often given in multiples of clock cycles.

2.4 FPGA

FPGA is short for **F**ield **P**rogrammable **G**ate **A**rray. For the new EF^{2}I readout system a Xilinx Virtex-7 FPGA is used, so the following section will be based on this device. More information about this device can be found in the following data sheets [13] and [14]. For other FPGA-devices, the functions may differ, but the basic principle is the same.

An FPGA is a programmable IC[10] for digital signal processing. It consists of input and output

[9] short for *analog to digital converter*

[10] short for *integrated circuit*

pins, different configurable logic parts, block RAM[11] and routing resources. In contrary to ASICs[12], the connections in an FPGA are not fixed. Because of this, FPGAs are often used to develop and evaluate a chip design, before the non-changeable ASIC is produced in large numbers. ASICs are hardwired and therefore less sensitive to radiation and other environmental influences compared to programmable FPGAs. With FPGAs logic signal data can be processed, in parallel and fast. For this different units as delays, registers, FiFos and calculation units are prepared. The programming of an FPGA is done in a hardware description language, normally VHDL or Verilog. The written code is processed in a synthesis and an implementation, which turns the code into an interconnection map for the logic parts in the FPGA. This is done with *Vivado*, a program by Xilinx. The program also ensures that the connections are not too short or too long, so that all processes within the FPGA run as simultaneously as possible and are compatible with the clock frequency.

In- and Output Pins A FPGA has several input and output pins (mostly in the order of 100 to 1000, depending on the model). Information about the IO's can be found in [15]. With these pins a digital signal can be led into or out of the FPGA. Most of the pins are *general purpose input/output* (GPIO) pins, meaning that they have no predefined function. The used pins have to be configured in the *.ucf*-file (for *Vivado*, the software included by the Virtex-7). In this file the digital standards with which the pin works are defined. There is also the opportunity to define pull-up or pull-down-resistors and a termination. Moreover, in this file a clock is defined, such that the FPGA has a reference value.

The pins can be configured as input or output pins or as inout pins, which makes them bidirectional. Some pins have a designated use, for example clocking pins, which can directly connect to the clocking network on the FPGA. This is important for distributing the clocking signal.

The pins support digital signals with different signal standards. The Virtex-7 FPGA has a maximal supply voltage of 1.8 V for the banks, meaning that the single-ended[13] signal standard must not exceed 1.8 V, whereby this e.g. is given for a LVCMOS18 standard. Differential[14] signals are often transmitted with an LVDS25 standard, which the FPGA also supports.

Clocking FPGAs have to get a clocking signal, on which the processes are synchronized and driven. The minimum and maximum frequencies depend on the FPGA model. A perfect clock is a square wave with a duty cycle of 50 %, which makes it a digital signal with the two alternating logic states: *high* and *low*. The slope should be infinitesimally small, so that no unwanted side effects like a jitter occur. *Vivado* provides a clocking wizard, which implements the clock from a single-ended or differential signal. It is possible to have multiple clocks with different frequencies and phase shifts. Inside the FPGA, the clock is distributed via a clocking tree to the clocked elements. In the best case, the clock signal arrives at all components at exactly the same time, which is optimized by routing over a clocking tree and arrange the elements at the appropriate time intervals. The clock skew is a measure of how well the routing worked in terms of time, as it indicates the greatest time difference between two signals. A clock can also drive just an IO-column, in which case it is not globally available and cannot drive e.g. a RAM, but it can drive the readout for an ADC.

[11] short for *random access memory*

[12] short for *application specific integrated circuit*

[13] Single wire signal transmission

[14] Double wire signal transmission, with two complementary signals, from which the difference is the effective signal, where disturbances are compensated.

FIFO FIFO is short for *first in, first out*. It is a storage, where the first element stored into it will be the first element, to be returned from the storage, so the order can not be changed[15].

A common usage of FIFOs is to change the clock domains. More, the incoming elements are synchronized to one clock frequency and the outgoing ones are synchronized to another one.

Block RAM In a BRAM[16] data can be stored in a discrete area inside the FPGA. The size of BRAM[17] depends on the FPGA-model. It can be used to store data, which is acquired during the processing of the FPGA, like read out data of an ADC. The data can be preloaded into the storage. The advantage of BRAM in contrary to a storage outside of the FPGA is its faster accessibility.

[15] The most important thing is to make sure, that the FIFO is not empty, when the readout starts, and it is not full, when one writes into it.

[16] short for *block random access memory*

[17] One block of RAM can not be splitted up into more, it has to be used all at once.

CHAPTER 3

Concept for Digitization

In the following, the concept for the chosen measurement technique of the filling pattern of the electron beam in the Stretcher ring will be explained. The aim is to digitize the signals of all four BPM electrodes in a similar, but faster way than the present setup, to deduce information about charge and position of the individual bunches. As a direct measurement of the BPM signals for characterization was not possible due to an accelerator upgrade, the first step was to simulate them. After the simulation results, the basic principle for digitization and how it is implemented in a measurement process will be presented in this chapter. For more detailed information about the used electronics and about the circuit boards, see section 4.

3.1 Simulation and Characterization of the Expected Signals

To estimate which specifications are required for the electronics, a output signal of one BPM electrode was simulated with the WAKEFIELD SOLVER of CST STUDIO SUITE[1].

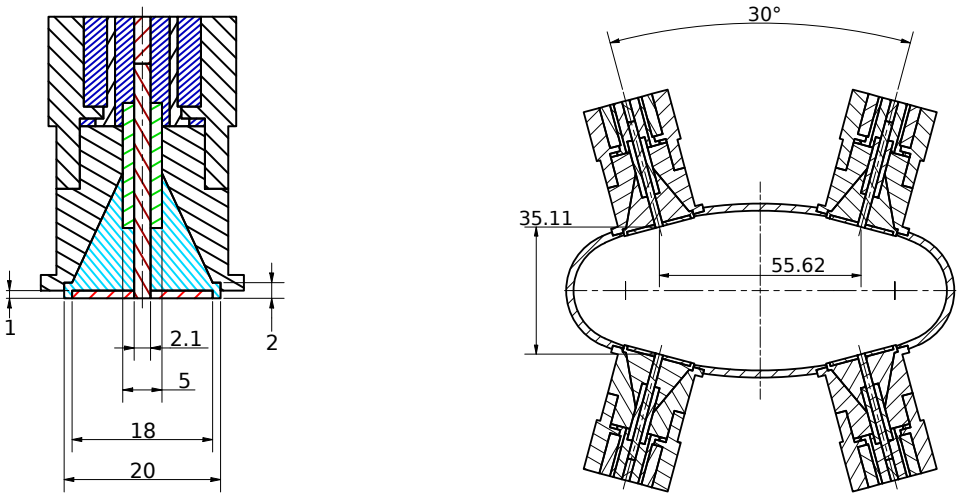
In the ELSA Stretcher ring both types of electrodes - DESY and ESRF - are installed. The working principle is the same, but for the DESY electrode, a 9 dB larger sensitivity and thus a larger output signal amplitude is expected, compared to the ESRF electrode (see [12, section 4.2.1]). Furthermore, the ESRF electrodes in the beam pipe are in use for the beam positioning system, while the DESY electrodes are not in use at the moment. Therefore, a DESY type BPM was selected as signal pickup. In figure 3.1, the technical drawings[2] of a DESY electrode and of a complete BPM, consisting of four of these electrodes, which are arranged symmetrically around the beam pipe, are shown.

In order to simulate the induced voltage signal on an electrode, the GAUSSIAN charge distribution of a bunch propagating through the centre of the BPM is simulated and solved by the WAKEFIELD SOLVER of CST STUDIO SUITE.

The simulation scenario with indicated electron propagation direction is shown in figure 3.2. Input parameters for the simulation are the speed of light as velocity, an overall bunch charge of $3.7 \cdot 10^{-11}$ C, as well as a bunch length of 15 mm. This bunch charge results in a beam current of approximately 19 mA, assuming that all bunches have equal charge. The bunch length corresponds to a typical bunch length at a total beam energy of approximately 1.7 GeV (see [11, section 4.2]). Both parameters are

[1] A program of Dassault Systèmes Simulia Corp., with which, inter alia, the field around a particle beam and electromagnetic interactions to nearby parts can be simulated. For more information, see [16].

[2] Because of insufficient information, these drawings can not assumed to be to scale.



(a) Technical drawing of a DESY-electrode.

(b) Technical drawing of the BPM.

Figure 3.1: The technical drawing of DESY-electrode (a) and BPM (b), which are used for the simulation of the voltage signal. The models were designed by Philipp Hänisch. The electrode consists of a conductive button electrode, with the button coloured light red and the feedthrough in dark red, a vacuum chamber (light blue), an air chamber (dark blue), an insulator (green) and the conductive housing (black). The top part of the stem can be used to simulate a resistor. All lengths are given in millimeters.

valid estimations in standard operation modes during productive beam times for the experiments. The simulated voltage signal between the electrode and the housing, which are connected via a resistor, and the corresponding FFT[3] can be seen in figure 3.3. From the simulated voltage, it can be deduced that the maximum amplitude is in the order of 100 mV. For a smaller bunch length or a higher bunch charge, the signal amplitude can become larger by approximately one order of magnitude. As for larger bunch lengths (compare equation 2.12) or reduced bunch charge, the signal amplitude decreases to 0 V, it is not reasonable to specify a minimum voltage. Nevertheless, the designed electronics (see chapter 4) has to cope with an input voltage range of several orders of magnitude. In addition, you can see in figure 3.3(a) that the signal has mostly decayed after about 1 ns. Since a bunch propagates through the BPM every 2 ns in the Stretcher ring, it is important that the signal of one bunch has completely decayed after 2 ns, so that it does not influence the next bunch. Only if this is the case, a single-bunch analysis is possible at all.

In order to design the appropriate signal processing electronics, it is crucial to know the bandwidth of the signal, i.e. the frequencies that occur and their share of the total signal. If the analog input bandwidth is chosen to small, higher frequencies in the signal will be strongly attenuated. This attenuates the total signal amplitude and the signal shape is distorted. With a Fast Fourier Transformation a time-discrete signal can be analysed due to its frequency dependence, which is shown in figure 3.3(b). Most of the frequency components are below 2.3 GHz, which results in a minimum analog input bandwidth of the electronics of 2.3 GHz.

[3] short for **F**ast **F**ourier **T**ransform: A algorithm to convert a discrete signal from time to frequency domain, so that it can be analysed according to the frequency components. This is implemented in SciPy [17].

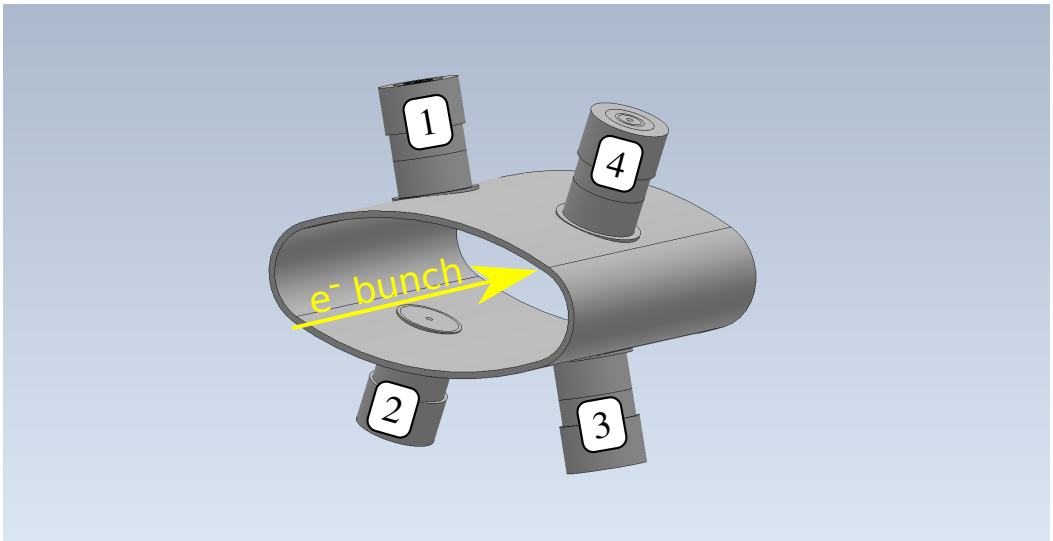
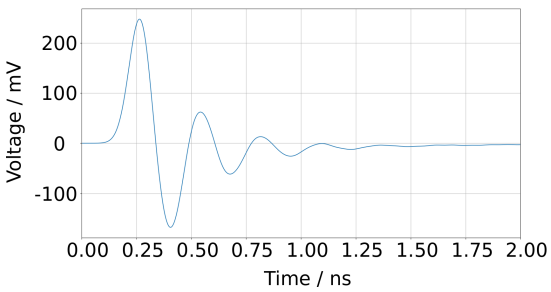
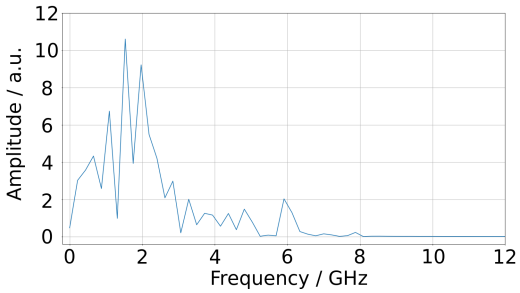


Figure 3.2: Simulation scenario of the BPM with the electron bunch propagating through the center. The materials used for the simulation are stainless steel for the beam pipe and the conducting parts of the electrode, alumina (Al_2O_3) for the isolator and vacuum as surrounding. The electrodes are numbered counter clockwise.



(a) Simulated voltage at one electrode of a BPM



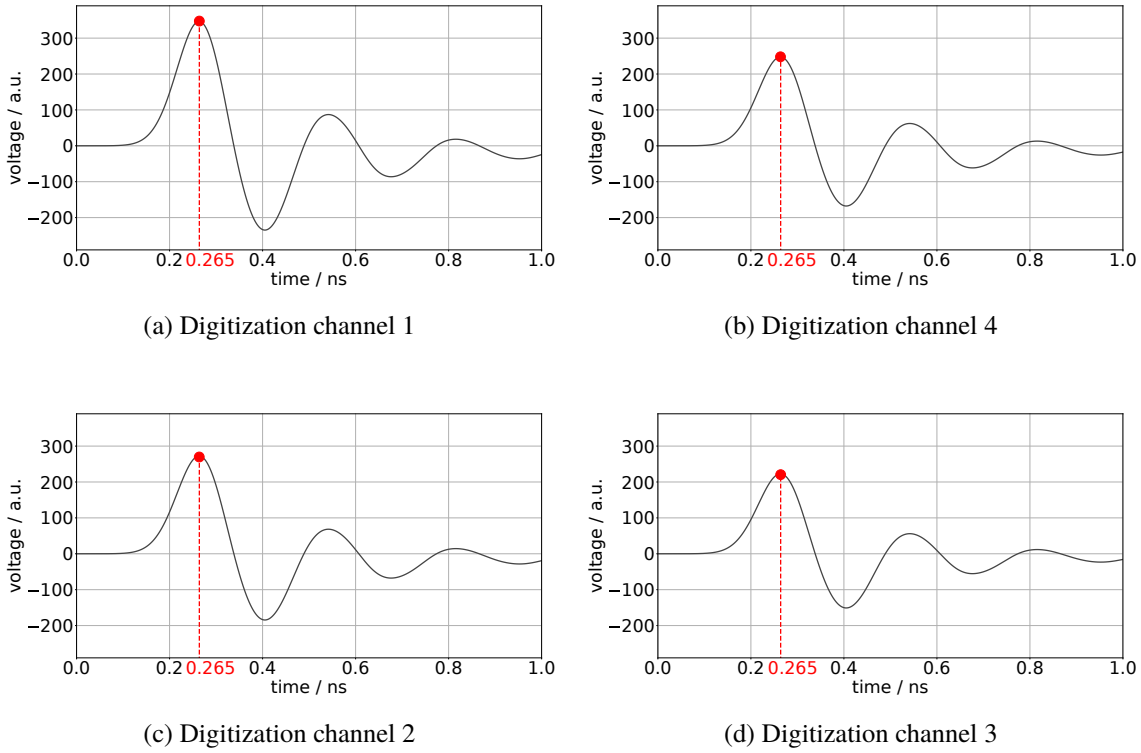
(b) Fourier transformation of the simulated signal

Figure 3.3: Induced voltage signal on a BPM electrode during the passage of a single bunch as it was simulated by CST with a bunch length of 15 mm and a bunch charge of $3.7 \cdot 10^{-11}$C. The simulated signal is shown on the left, the corresponding Fourier transformation is shown on the right. The data was Fourier transformed using SciPy [17].

3.2 RF-Synchronous Digitization

For further digital processing of the BPM signals, they have to be digitized. To determine the spatial position of one bunch, it is sufficient to get one sampling point per bunch passage on each of the four BPM signals at exactly the same time (the signal must of course be different from zero). From these four samples the bunch position can be deduced as described in 2.2.1. The optimal point in time for the digitization coincides with the maximum amplitude of the induced voltage signal.

In this case, the signal-to-noise ratio is as large as possible and the amplitude of the signal has the largest absolute value. Additionally, the derivative of the signal is zero at its maximum, so the



(a) Digitization channel 1

(b) Digitization channel 4

(c) Digitization channel 2

(d) Digitization channel 3

Figure 3.4: The simulated electrode signal is drawn in grey and is only used for orientation at which position of the signal the optimal sample point is located. The sampling point and value are shown in red at the optimal time for all four electrodes to determine the bunch position.

digitization at this point in time is less sensitive to unavoidable timing jitter of the electronics.

In figure 3.4, the optimal sampling point in time is depicted for all four electrode signals. In this case, the beam was simulated not to be centred in the beam pipe, but shifted to the top left, resulting in a larger maximum amplitude of the signal in top left electrode 1 compared to the signals at the other electrodes. The expected signal curves have been drawn in grey. However, the sampling is done only at one point of the waveform. The red dots show the optimal digitization points, which occur at the same sampling time for each electrode.

For this measurement to function, the bunch must not oscillate longitudinally and the maximum must be constant in time for all bunches. The expected position of the maximum without oscillation effects depends only on the bunch length (see equation 2.15). The bunch length at fixed momentum compaction factor and fixed synchrotron frequency is linear dependent on the beam energy (corresponding to equation 2.11). The fixed reference point in time, provided by the acceleration frequency from the master generator, and the time the bunch passes through the BPM is constant a long as the above accelerator settings remain constant. Furthermore, there are two types of longitudinal bunch oscillations. On the one hand, incoherent synchrotron oscillations, where electrons oscillate within the bunch. These are unavoidable, but negligible as there are many electrons in a bunch, because the oscillations are incoherent and therefore are averaged out. On the other hand, there are also coherent

synchrotron oscillations in which the bunch oscillates as a whole, i.e. all electrons oscillate in phase. With this, the problem arises that the centre of charge of the bunch is oscillating and thus the delay between the reference point in time and time, where the bunch passes through the BPM, is not constant. To dampen these oscillations, a bunch-by-bunch feedback system is installed in the Stretcher ring so that their oscillation amplitude become negligible and the delay is kept constant. It follows that the maximum amplitude of the signal induced on the electrode, in case the bunch-by-bunch feedback system is switched on and as long as no accelerator parameters are changed, has a constant delay to the 500 MHz signal of the master generator[4], enabling a synchronization of the sampling to it

As the sampling time is deducted from the master generator signal, the position of the maximum has to be determined in reference to it, to adjust the delay for the optimal sampling time. In figure 3.5, the measurement principle for this adjustment of the delay is shown. To do this, the signal of one electrode is split up into four equal signals and each is sampled with one of the four ADCs (see section 3.3) at slightly different sampling times. Since the same signal was digitized, the points can be drawn in one diagram and the course of the signal becomes visible. A function, similar to equation equation 2.15, can be fitted to the waveform to determine the maximum.

For a measurement of the bunch charge, there are two options: an absolute measurement and a relative one. For an absolute measurement according to equation 2.15, all proportionality factors and the exact sampling time have to be known. In reality, these variables are hard to determine. Additionally, the exact geometry of the BPM electrode is unknown, so only a relative measurement is suitable.

3.2.1 Calibration of the Relative Bunch Charge

The overall averaged current in the Stretcher ring is measured by a Bergoz current monitor. From the current of the beam follows

$$\mathrm{I_{beam}} \propto \mathrm{Q_{beam}} = \sum_{i=1}^{n} \mathrm{q_{b,\,\mathit{i}}} \tag{3.1}$$

with the charge of the whole beam $\mathrm{Q_{beam}}$ and the bunch charges $q_{\mathrm{b},\,i}$. From this follows

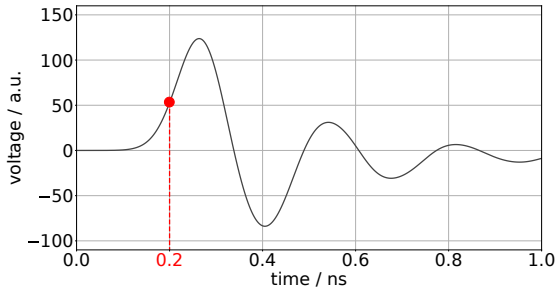
$$k \cdot \sum_{i=1}^{n} \mathrm{q_{b,\,uncal,\,\mathit{i}}} = \mathrm{Q_{beam}} \tag{3.2}$$

with a calibration factor k and the measured, uncalibrated values for the bunch charges $\mathrm{q_{b,\,uncal,\,i}}$. The charge $\mathrm{Q_{beam}}$ of the whole beam can be calculated by

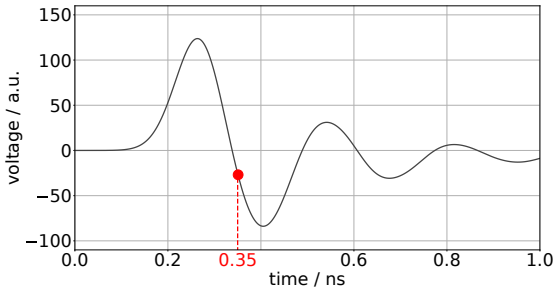
$$\mathrm{Q_{beam}} = \frac{\mathrm{I_{beam}}}{\tau_{\mathrm{rev}}} \tag{3.3}$$

with the revolution time τ_{rev}, which is approximately 548 ns in the Stretcher ring. Because $\mathrm{Q_{beam}}$ can be calculated, the calibration factor k can be determined. This leads to the fact that the measured

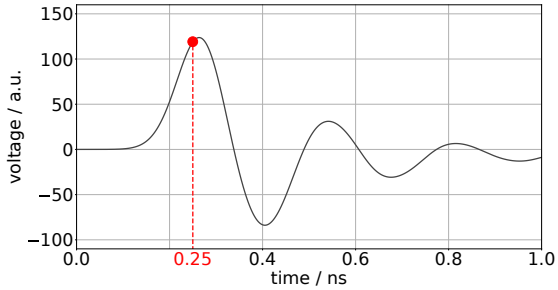
[4] This frequency generator generates the signal for the acceleration frequency in the Stretcher ring and the Booster synchrotron and the timing system. The acceleration frequency, which is also the sampling frequency, is assumed to be 500 MHz, although it is actually 499.668950 Hz.



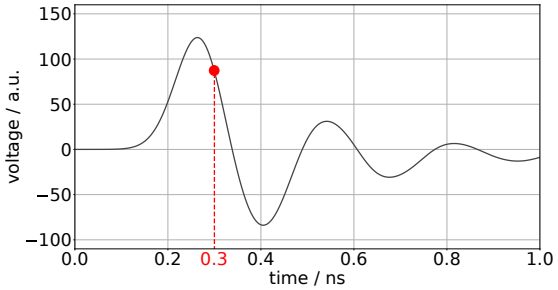
(a) Digitization channel 1



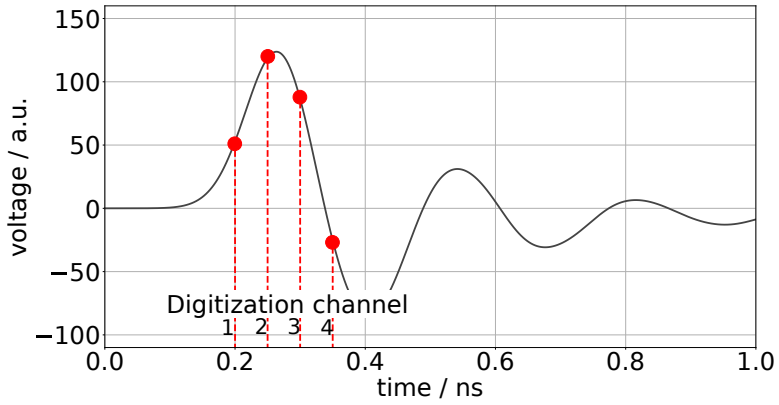
(b) Digitization channel 4



(c) Digitization channel 2



(d) Digitization channel 3



(e) Sample points of all digitization channel in one diagram

Figure 3.5: The expected signal for orientation is drawn in grey and the sampled values in red. The signal of one BPM is split up, so that each ADC samples the same signal at a slightly different time, shown in (a)-(d), and the single sampling values of the digitization channels can be add up into one diagram (e).

bunch charges can also be calibrated

$$q_{\mathrm{b,\,uncal},\,i} \cdot \frac{1}{k} = q_{\mathrm{b},\,i}. \tag{3.4}$$

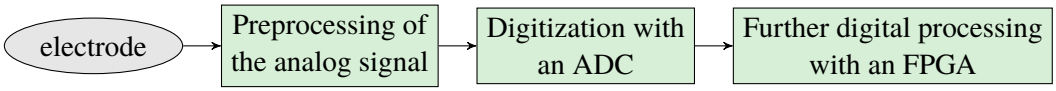


Figure 3.6: The analogue signal, which is induced onto the electrode, is preprocessed in a first stage and than digitized with an ADC in the next stage. The digital signal is further processed with an FPGA.

Since I_{beam} varies in the booster mode –the mode in which the accelerator is normally operated for the experiments –the calibration factors for the different beam currents must be determined and stored during operation in Syli mode. Due to the sensitivity of the calibration factors on the sampling time, first it has to be ensured that the sampling takes place at the maximums signal amplitude.

3.2.2 Splitting of the Bunch Charge Measurement Procedure

Due to electronics and cable delays, which may differ for instance with temperature fluctuations, and accelerator specific parameters like the beam energy or the acceleration phase, which can be set, the point in time of the maximum amplitude is not fixed. Therefore, a constant adjustment of the timing delay is necessary. This leads to two different parts of the measurement procedure:

- Amplitude Measurement → Quasi continuous determination of charge and position of each bunch
- Sampling Time Adjustment → Determination of the optimal sampling time of the maximum amplitude of the bunch signal relative to the clocking signal, coming from the master generator, and subsequently adjustment of the delay between BPM and clocking signal.

The sampling time adjustment is essential to perform the amplitude measurement, which than provides information about spatial position and charge of the bunches.

3.3 Amplitude Measurement and Sampling Time Adjustment

In this section the implementation of the key concepts, introduced in section 3.2, in a measurement procedure is presented.

Amplitude Measurement For the amplitude measurement, the signal should be digitized by an ADC at the point in time where the amplitude is largest for all four electrodes of a BPM. Four digitization channels that are structured the same way are required for this. The channels can be split up into three stages of signal processing (see figure 3.6).

For all four channels, the signal processing path is outlined in figure 3.7, where the different stages are drawn in green.

To exhaust the full dynamic range of the ADC the signals coming from the BPM are attenuated or amplified in a first stage. Here, a variable gain that can be adapted to the amplitude of the input signal is chosen. If signals with larger amplitudes then expected in a measurement scenario are generated, a preattenuator is provided as a precaution to protect the following electronics, which can be switched on, if required.

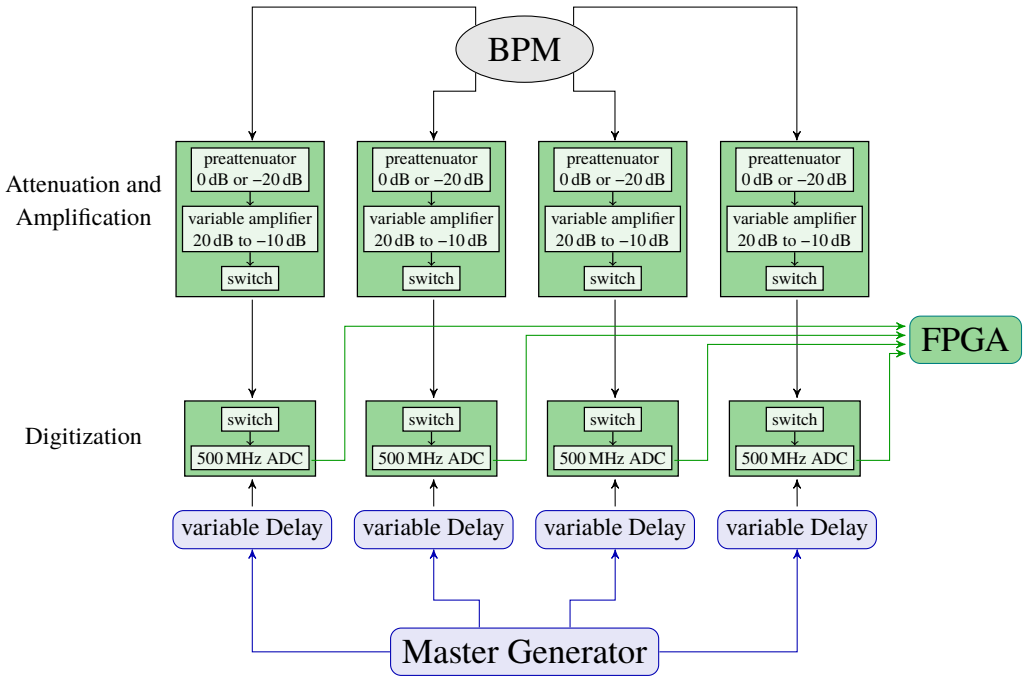


Figure 3.7: Equivalent circuit diagram of the digitization process. The four BPM electrode signals can be digitized at the same time with four equal digitization channels. The ADC is read out with an FPGA. To avoid damage on the electronics and to exploit the whole sampling range of the ADC, there are attenuators and an amplifier included.

In the next stage, the digitization process takes place. For this a fast sampling ADC (an ADS54RF63 by Texas Instruments [18]) was chosen. It has a maximum sampling rate of 550 MHz, which is slightly higher than the rate at which the sampling is done. The differential input should not exceed 2 V peak-to-peak. The input bandwidth is given with 2.3 GHz. In the FFT diagram in figure 3.3(b) can be seen that most of the frequency components are less than 2.3 GHz, so this ADC's bandwidth is sufficient to sample the signal. The ADC has a resolution of 12 bit. Additionally, one indicator bit for overrange (OVR) detection of the analog input signal. The sampling is synchronized to the clock input, which will be provided by the master generator. Thus, the synchronicity to the BPM signal is guaranteed. The digitization process takes a fixed amount of time, so the ADC provides a data ready (DRY) signal, which is synchronous to the 13 bit (12 bit resolution and the OVR bit) data signals and shows a fixed delay to the point in time where the data on the outputs are valid and available for further digital signal processing. As the DRY signal toggles from logic 0 to 1 and vice versa (see datasheet [18]), it can be used as a digital clock signal with half of the rate of the input sampling clock (250 MHz in this case).

An FPGA, where the further processing of the digital signal takes place, is the final stage. For this the VC707 evaluation board by Xilinx [13] with a Virtex-7 FPGA (XC7VX485T) was chosen. With the FPGA, the data from the ADC can be read out, preprocessed, buffered and sent to a PC for storage and visualization of the filling pattern. In addition, the gain and the switches can be controlled with the FPGA.

Sampling Time Adjustment In this measurement, the signal of one single electrode is to be digitized with all four ADCs. Since the stages are the same as for the amplitude measurement, the same channels can be used. For this, it must be ensured that in the first step the amplified signal is split up and reaches all four ADCs. Therefore, the interconnection between the Attenuation and Amplification Stage and the digitization stage is altered using the switches, enabling the transfer of the signal of one BPM electrode to a splitter, where this signal is split up into four equal signals and subsequently is delivered to all four ADCs, as seen in figure 3.8.

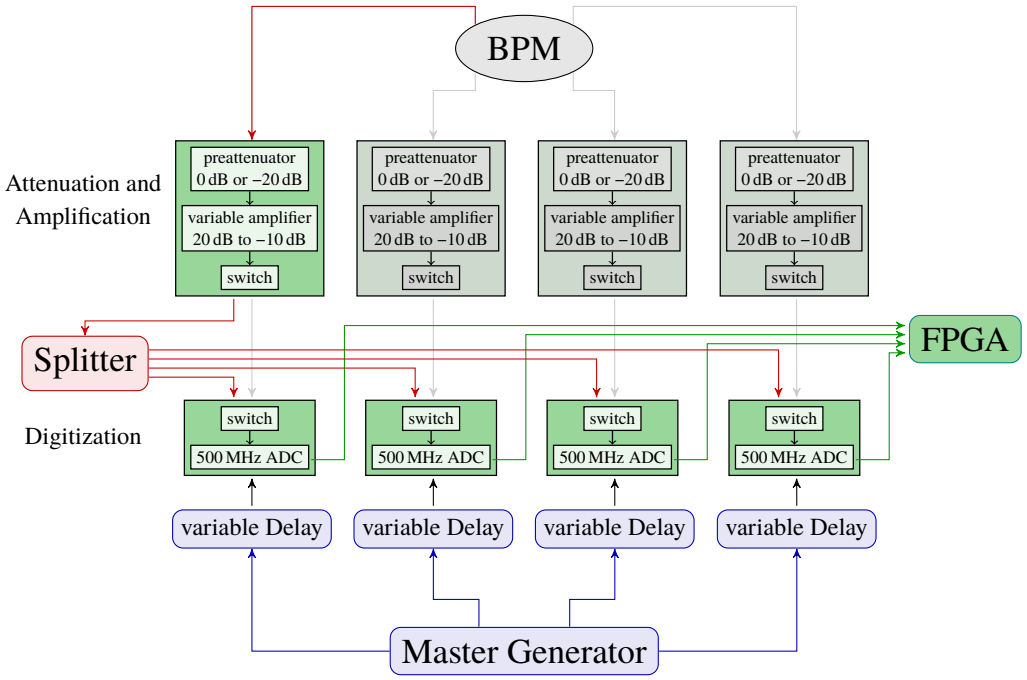


Figure 3.8: Equivalent circuit diagram of the digitization process for the phase measurement. In this case, the switches redirect the circuit to the power splitter, so that each of the ADCs gets the signal of the same electrode.

The delay between the individual digitization channels is adjusted the way that the time difference of the sampling between them is in the order of 50 ps, as the maximum extends to approximately 200 ps, enabling the measurement of four consecutive sampling points of the signals waveform. These four points per bunch signal can be fitted with a function proportional to equation 2.15, so that the delay can be adjusted such that the sampling during the Amplitude Measurement takes place at the maximum of the signal waveform.

CHAPTER 4

Electronics for Digitization

In order to convert the concept, which was presented in chapter 3, into a measuring system, several circuit boards[1] were designed during this thesis. In the following, the individual boards are presented and what particular attention was paid to during the design phase.

4.1 General Design Information

To design the circuit boards, the software *eagle* [2] by *autodesk* was used. With this software a circuit diagram can be created and the circuit board can be routed following the diagram. The software takes care that the board has been routed as drawn in the circuit diagram and that the design conforms to the constraints defined by the manufacturer.

For the routing, a distinction was made between four different types of signal, which have different requirements in terms of width and separation and the conducting tracks. The different signal types are:

- Single ended high frequency analog signals (i.e. BPM signals)
- Single ended low frequency digital signals (i.e. control signals for switches and attenuators)
- Differential high frequency analog and digital signals (i.e. the output signals of the ADC, preprocessed BPM signals and clock signals)
- Power supply.

For high frequency signals it is inevitable to choose the track in a way that the impedance is 50 Ω and 100 Ω, respectively.

For the track, common layouts are a microstrip, where the track is located on a ground plate, and a stripline, where the track is enclosed between two ground plates. These two types of tracks for a single-ended and a differential signals are sketched in figure 4.1.

The stripline design has more precise electrical characteristics, because here the signal track is enclosed between the two ground plates shielded against environmental influences. The design is often

[1] Also called PCB, short for *printed circuit board*.

[2] short for **e**asily **a**pplicable **g**raphical **l**ayout **e**ditor

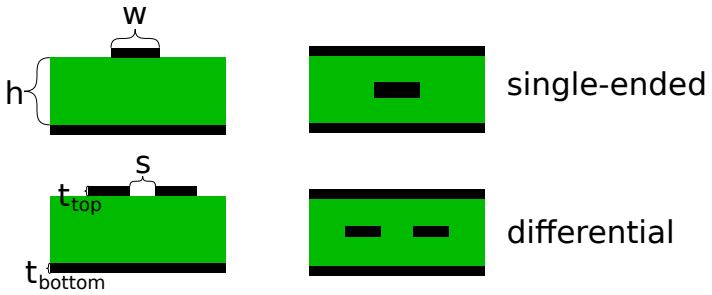


Figure 4.1: On the right side one can see embedded tracks between two ground plates, on the left side are surface microstrips on one ground plate. In green the prepreg is imaged.

used when several signals are routed on top of each other in a board, when the signals are particularly susceptible to electrical interference or when there are strong sources of interference in the vicinity of the board. The additional ground plates make the board thicker and more expensive to manufacture. Therefore, microstrips where chosen, because there is no need for more than four layers and the constraints regarding the thickness of the prepreg[3] as well as the thickness of the copper layer are less restrictive. Because the pregrep and copper thickness is specified by the manufacturer, the width of the track and, for differential signals, the distance between the tracks has to be determined, which is possible by an impedance calculator[4] as a first approximation. The values for the thickness and the effective relative permittivity ϵ_r of the prepreg vary due to the manufacturing process, which has impact on the calculated track width. For clarification, a testing board (see section 4.1.1) with different track widths was designed. The influence of different solder pad sizes for resistors and capacities, the geometry of the track and the influence of grounded vias[5] next to the track were also tested.

For the power supplies no specific impedance matching is required, here care should be taken that there is minimal ohmic resistance and power dissipation, so wider tracks should be used.

4.1.1 Testing Board

For testing and comparison of different possibilities to design a track, a testing board was designed. The testing board is a 4-layer board, manufactured by Multi-CB.

The testing board can be seen in figure 4.2. In order to save space, both top and bottom layer were used for the testing tracks. All tracks are surface microstrips with different characteristics, like vias[6] next to the track, soldered 0 Ω resistors with different case sizes or different geometries, which are specified in the appendix, table A.1.

To measure the characteristics, especially with regard to the impedance of the different tracks a Vector Network Analyser (VNA) was used. With this device an analysis of reflection and transmission of signals at different frequencies can be performed. The device emits pulses at different frequencies with a specific power and subsequently measures the reflected or transmitted power. The device can also conduct a TDR[7] measurement, in which it is possible to measure the position dependent

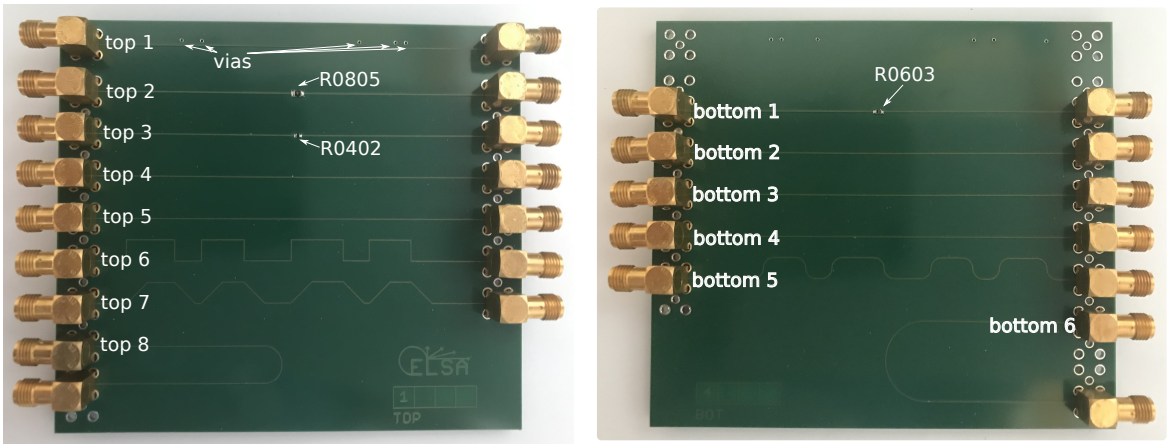
[3] short for *preimpregnated fibers*

[4] The impedance calculator of Multi-CB [19], the manufacturer of the PCBs.

[5] Electrical interconnection between different layers of the PCB.

[6] A via is a electric interconnection between different layers of the PCB.

[7] short for *Time Domain Reflectometry*



(a) Top side

(b) Bottom side

Figure 4.2: Top and bottom side of the testing boards. There are different geometries and widths of the tracks. The board consists of 4 layers including two plates connected to ground in the middle to achieve the same surface microstrip structure on top and bottom side. It was manufactured by Multi-CB.

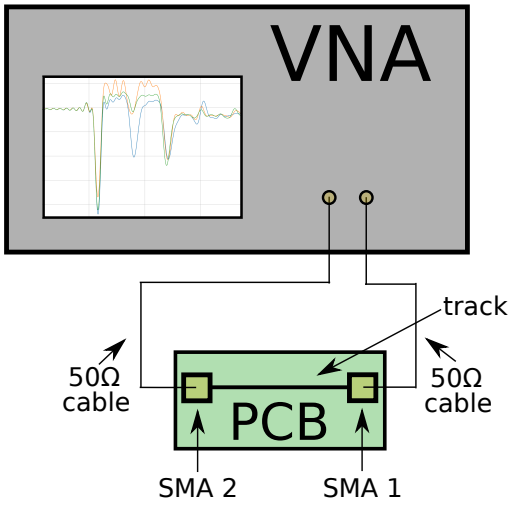


Figure 4.3: Sketch of the measurement setup.

impedance of e.g. a track on a circuit board. Due to the measuring method, the absolute values of the measurement can not be assumed to be accurate, however, it can be used to distinguish different impedances and rapid impedance changes. To evaluate the board, it is connected to the VNA as shown in figure 4.3. In the sketch, one can see a track of the test board with an SMA connector SMA 1 on the right side and SMA 2 on the left side. The SMA connectors are each connected to the VNA via a 50 Ω cable of different length.

In figure 4.4, the result of TDR measurements of the tracks top2, bottom1 and top3 of the testing board (see figure 4.2 and table A.1) can be seen. All three tracks have the same track width and length, an SMA connector on both sides and a 0 Ω resistor in about the middle of the track. However, the

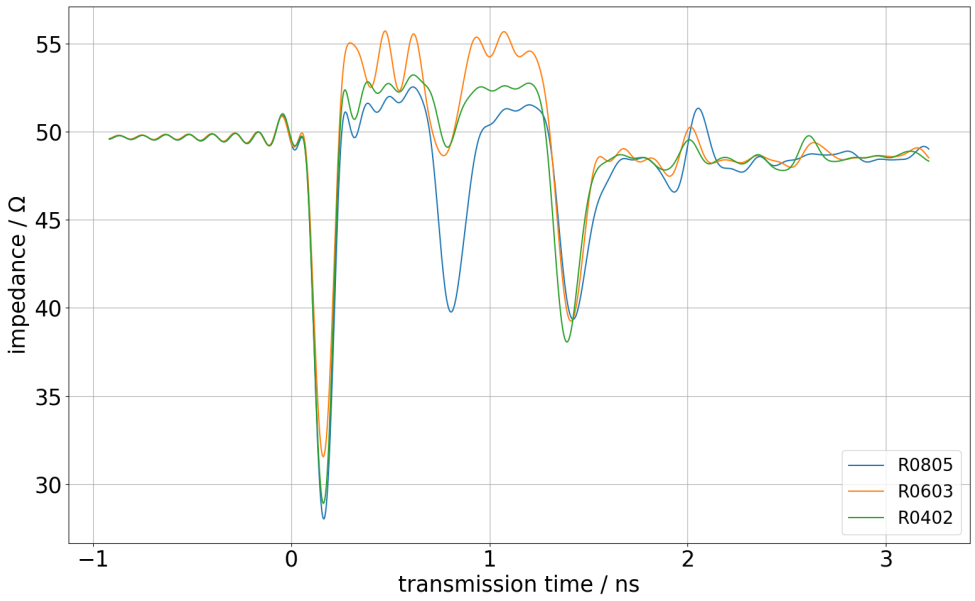


Figure 4.4: A TDR measurement of the testing board for three different pad sizes connected with corresponding resistors.

SMD-resistors are of different sizes[8] as shown in table A.1 and so the soldering pads are also different in size. On the x-axis the transmission time and on the y-axis the impedance is shown. From the transmission time, the position on the track can be determined. The VNA was calibrated to show t = 0 ns at SMA connector 1. For all tracks one can see the SMA connector SMA 1 at the beginning of the board with a impedance variation at time 0.2 ns and SMA 2 at the end of the board with another impedance variation at time 1.5 ns. The corresponding peaks of SMA 2 appear smaller, due to the measuring technique. The measurement becomes less precise if a large amount of the signal is already reflected before this point. If the measurement is performed with swapped connections, the SMA 2 appears with a larger jump of the impedance, what shows, that the difference in impedance change at the SMA connectors is a measuring artefact. Nevertheless, it can be seen that the jump of the impedance between track and resistor is smallest for size R0402 (green data) and largest for size R0805 (blue data). Consequently, resistors and capacitances of size 0402 were used for high-frequency tracks.

Due to ambiguous results for the different track widths (see appendix A.1), a track width of 230 µm for single ended and 134 µm with a distance between the two tracks of 125 µm for differential signals was chosen. In addition, care is taken to ensure that curves have as large bending radii as possible and that there are no sharp angles in the track (results can be found in the appendix A.2 and A.3).

[8] The casing size is given in length times width in *inch*.

4.2 PCBs of the EF^{2}I System

In the following, the circuit boards that were designed and manufactured for the EF^{2}I system are presented. Figure 4.5 shows all boards and how they are connected.

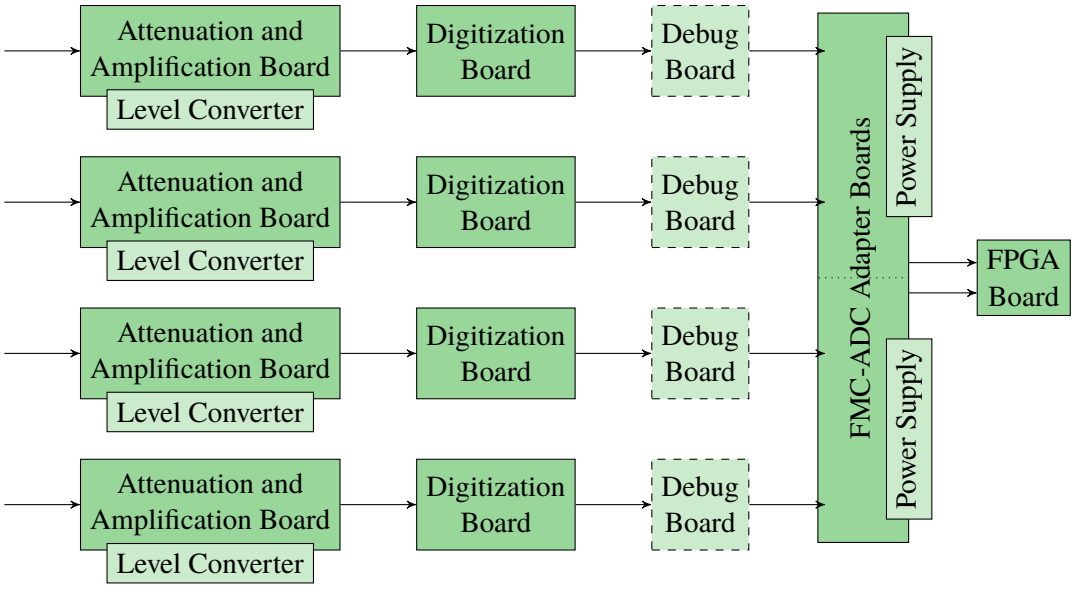


Figure 4.5: Block diagram for interconnection of the individual PCBs.

4.2.1 Attenuation and Amplification Board

As explained in section 3.3, the BPM signals are preprocessed on the Attenuation and Amplification board. The board can be seen in figure 4.6. For each of the four channels corresponding to the four BPM electrodes, one board is required. The same board fits to all four channels. Based on the results of the testing board (see section 4.1.1), a higher quality PCD End Launch Jack type SMA connector was chosen to reduce the signal amplitude loss by reflection at the SMA connectors.

The first element in the analog preprocessing chain is an attenuator of the type HMC802ALP3E [20] by Analog Devices with an attenuation of 20 dB, which can be switched on and off by an one bit logic signal. The corresponding control signal from the FPGA is level shifted from 1.8 V to 3.3 V to satisfy the required input level of the attenuator (see section 4.2.1). Further, an ADL5243 by Analog Devices [21] is used for a variable amplification or attenuation of the BPM signals. The IC consists of a variable attenuator with a maximum damping factor of −31.5 dB which can be changed in 0.5 dB steps, where the output is connected to a fixed amplifier of 20 dB. With the attenuator followed by the amplifier, the dynamic range is enlarged as large signals are attenuated first, so that the amplifier does not saturate as quickly. There are also level shifted signals from the FPGA used to control the 6 bit variable adjustable attenuator. To change between the four outputs, a four channel high frequency switch ADRF5040 by Analog Devices [22] is used. Although only two output ports are needed, four were prepared so that there is more flexibility for future extensions. Both ICs are soldered to a ground plate for better cooling.

The board was evaluated with the Vector Network Analyzer (VNA). To do this, the input port and the port to be measured were connected to the two ports of the VNA in each case, as shown in figure 4.3. The input power was set to 0 dBm, the attenuator was set to 0 dB and the fixed amplifier amplifies the signal by 20 dB, which results in an effective amplification of 20 dB (not taking insertion losses of the IC and of the board into account). The measured output powers for all four output ports for a certain frequency range are shown in figure 4.7. It can be seen that two output ports of the board differ from the other two, so care should be taken that the same output ports of all four boards are used in the further application. Up to 2 GHz the power level almost stays constant. From 3 GHz, the attenuation increases rapidly. For frequencies higher than 4 GHz the attenuation becomes so large, that the signal to noise ratio is too small to measure the output power accurately. As seen in section 3.1 figure 3.3(b), it is not to be expected that the analog input signal of this board, which is the induced bunch signal from the BPM, will have dominant frequency components higher than 3 GHz.

For the following comparison of the different attenuation levels, which can be switched on separately, of the variable attenuator as well as the separated 20 dB preattenuator, output channel four of the board was used. For the measurement with the VNA, input port and output port four are connected to the VNA. On the one hand, as seen above, there are attenuations from the board itself and, on the other hand, the fixed amplifier can not be switched off, so a normalization measurement is done first. For this, the effective amplification of the board was set to 20 dB, comprising the fixed 20 dB amplifier and additional 0 dB from the attenuators. The input power was again set to 0 dBm. The measurement series is plotted in blue in figure 4.8. This normalization measurement is taken as the base line, so all other measurement series have been subtracted from it. The normalized data of the other series of measurements for the various individually enabled attenuation (−1 dB, −2 dB, −4 dB, −8 dB, −16 dB, −20 dB) levels are also shown in figure 4.8 and the corresponding ideally expected result is drawn as horizontal grey lines. It can be seen that the various gain levels for low frequencies correspond almost exactly to the expected values. An oscillation around the expected value, as seen for large attenuations and higher frequencies, indicates that the signal could not be measured properly, because

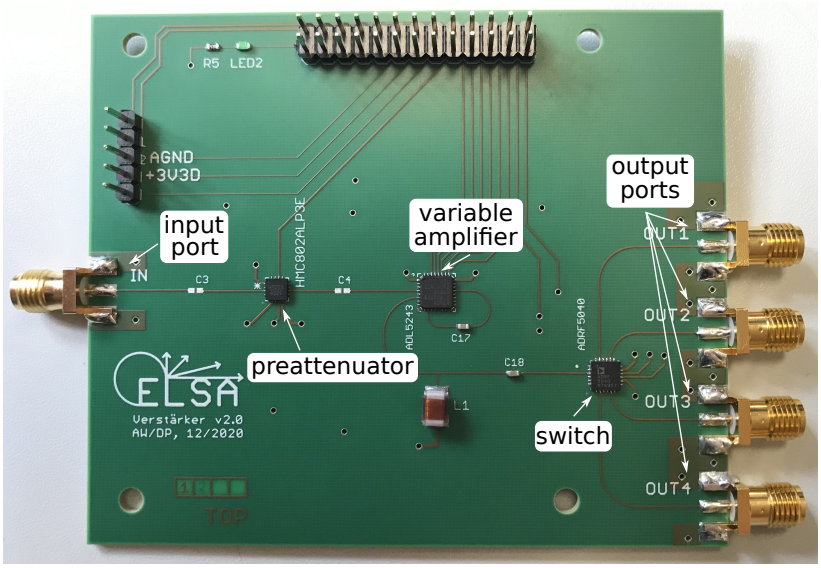


Figure 4.6: Photo of the Attenuation and Amplification board

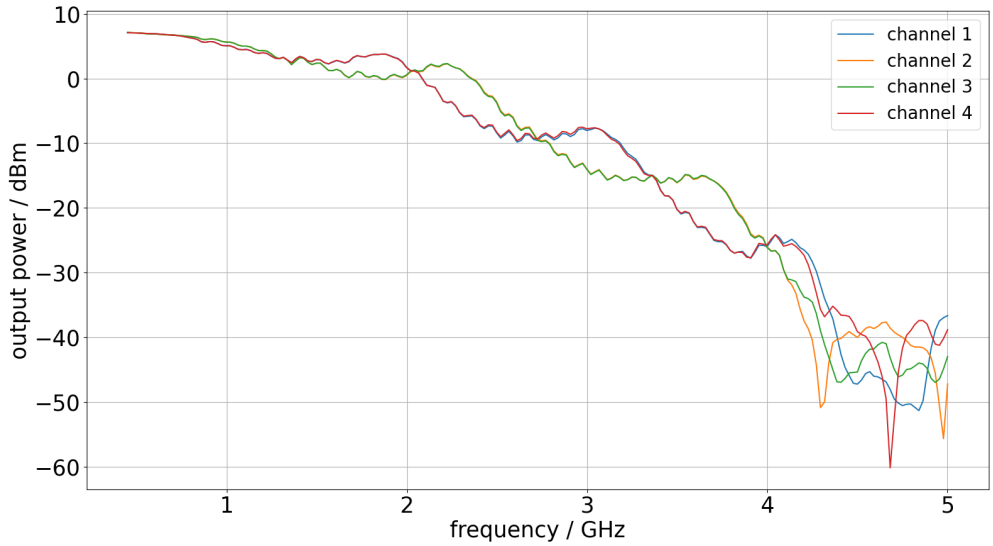


Figure 4.7: Output power of the Attenuation and Amplification board in dependence of the frequency for the four channels.

the signal-to-noise ratio becomes smaller. Up to the minimum required 3 GHz the attenuation levels correspond to the expected value and the attenuation is not frequency-dependent.

Level Converter

Because the FPGA is only able to generate output signals up to 1.8 V, a level converter is needed for the ADL5243 and the HMC802ALP3E. The board[9] is shown in figure 4.9. On this board the power supply, the control signals for the switch and two additional signal tracks are only passed through. The logic signals for both attenuators, however, are routed through an Level converter (SN74LVC8T245 [23]), converting the level from 1.8 V to 3.3 V. The board was designed to act as a reverse level converter from 3.3 V to 1.8 V as well.

4.2.2 Digitization Board

Within this master's thesis, a Digitization board was designed and after evaluation further improved.

Version 1

The first version of the Digitization board is shown in the appendix, figure B.1.

The main IC is a 550 MHz sampling ADC, an ADS54RF63 [18] by Texas Instruments. The ADC expects a differential clock signal (LVDS[10]). Thus, the analog single-ended sinusoidal clock signal provided by the ELSA-HF master generator is converted using an LVDS compatible comparator.

[9] designed bei Dennis Proft

[10] short for **L**ow **V**oltage **D**ifferential **S**ignaling, which is a serial signalling standard for high frequencies.

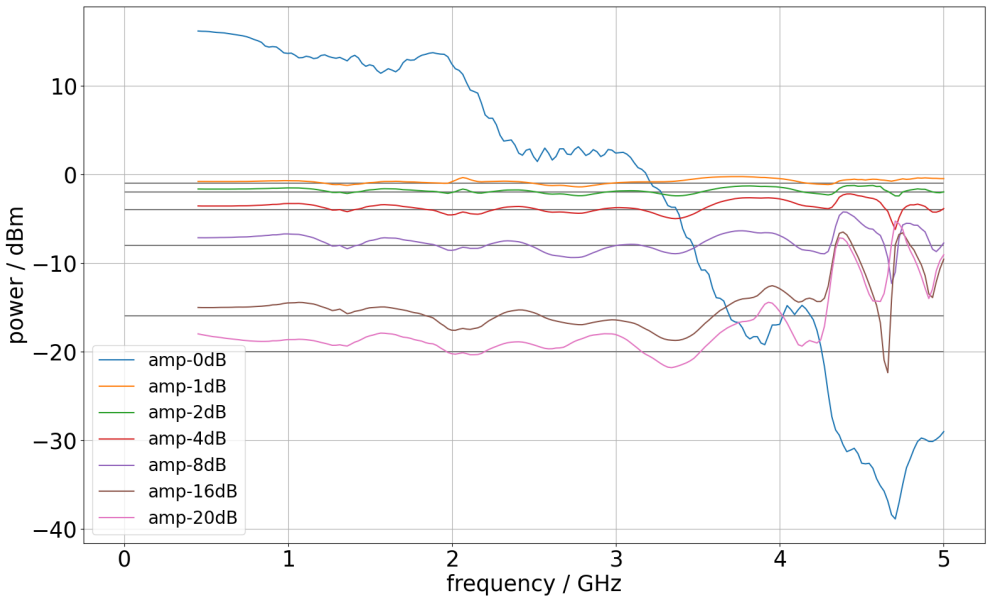


Figure 4.8: Measurement to verify the values of the different attenuation levels. The data for the baseline is plotted in blue. Every attenuation level is subtracted from the base line.

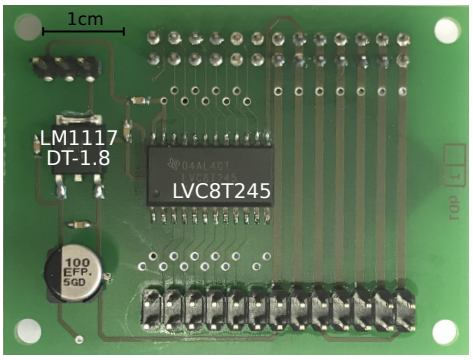


Figure 4.9: Photo of the level converter board

An additional PLL[11], a SI5317A [24], was installed to minimize the jitter on the clocking signal. During the development it turned out, that the additional PLL does not improve the jitter significantly and has disadvantages due to its opaque controls, so it was removed from the board for the second version (see below). The board is equipped with four input ports for the signal to be sampled. With a switch, which is identical to the one on the Attenuation and Amplification board, it can be selected which input port is routed to the ADC.

For the ADC, the single ended input signal has to be transformed into a differential signal, which is achieved with two 1:1 transformer (L2 and L1 on the board [25]).

[11] short for *phase-locked loop*, a phase stabilizer

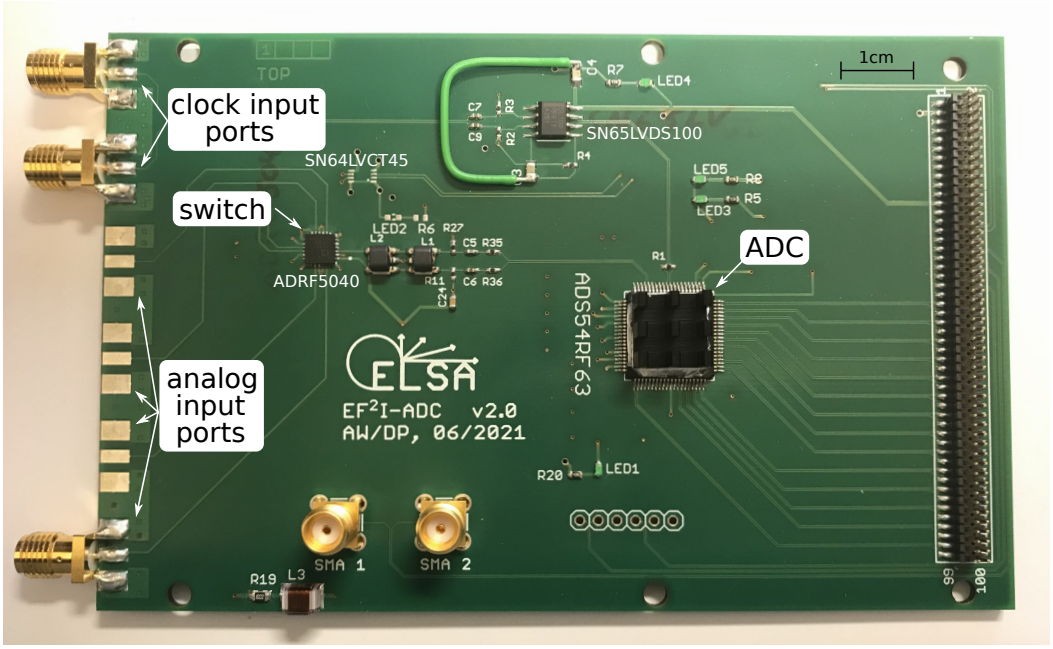


Figure 4.10: Photo of the second and final version of the Digitization board

For the connection to the FMC-ADC Adapter board, a 100-pin connector by Samtec (FTSH-150-01-F-DV) is used and the SMA-connectors are the same as for the Attenuation and Amplification board.

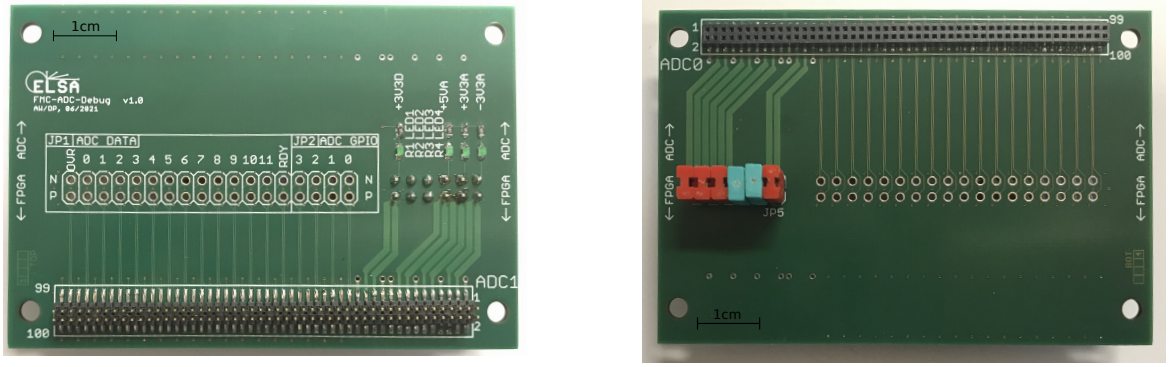
A distinction was made between an analog ground and a digital ground, each of which is connected to the associated voltage supplies and signal inputs. The separation of the grounds ensures that the analog input signal to be sampled, which is in reference to the analog ground, is not influenced by rapid changes in potential of the digital ground. The two grounds are connected for low frequencies via inductance L1 and resistor R19, with the high-frequency interfering part being filtered out by the inductance.

Version 2

The second version of the Digitization board is shown in figure 4.10.

The innovations are:

- A single-ended to differential converter (SN65LVDS100 [26])
- A buffer (SN74LVC2T45 [27]) between FPGA and Switch
- More space between ADC and Samtec-connector, to enable a better cooling of the ADC
- An LED on each power supply to indicate its working status



(a) Top side

(b) Bottom side

Figure 4.11: Photo of the top and the bottom side of the Debug board

FMC-ADC Debug Board

A debug board[12], which can be seen in figure 4.11, can be connected between Digitization and FMC-ADC Adapter board. The purpose of the board is to test the ADC output and to switch the power supply for the Digitization board on and off individually. It offers test pads for all 14 differential signals of the ADC for debugging of the communication between ADC and FPGA.

4.2.3 FMC-ADC Adapter Boards

The FPGA GPIO pins are connected to two FMC-HPC connectors on the FPGA board. For these, an adapter board with an FMC-HPC connector is designed to interconnect the GPIO pins to the Digitization and the Attenuation and Amplification board. The adapter boards[13] can be seen in figure 4.12.

Two different boards are needed, because the FMC-HPC pin layout differs for both connectors at the FPGA board. The adapter board on the left side has more additional user pins, which are not used yet. The connectors for the Digitization boards (CLP-150-02-F-D) are all occupied equally. Each of the FMC-ADC Adapter boards is equipped with a power supply board. From here the power is distributed to the Digitization and to the Attenuation and Amplification boards.

Power Supply Board

For the Digitization boards and the Attenuation and Amplification boards different voltages are required: 5 V, 3.3 V and −3.3 V in regard to the analog ground and 3.3 V in regard to the digital ground. All voltages are generated from a single 7 V power supply using low drop linear voltage regulators and DC/DC converters. The board[14] is shown in figure 4.13.

[12] designed by Dennis Proft
[13] designed by Dennis Proft
[14] designed by Dennis Proft

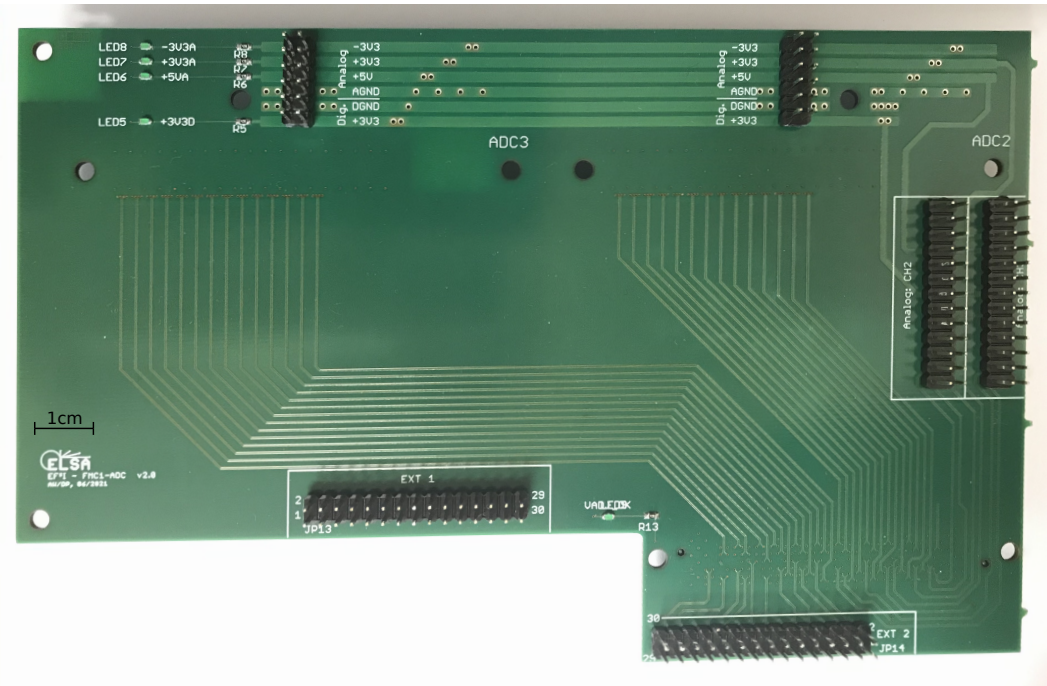


Figure 4.12: Photo of the top side of the left FMC-ADC Adapter board

4.3 FPGA

The Xilinx FPGA was purchased from Xilinx on a finished evaluation board, which is briefly described in subsection 4.3.1. The configuration of the FPGA is dealt with in subsection 4.3.2.

4.3.1 FPGA Board

As FPGA board, a VC707 evaluation board by Xilinx [13] with a Virtex-7 FPGA (XC7VX485T), as mentioned in section 3.3, was chosen.

The board has an interface for USB and Ethernet. It can be programmed directly via PC using the Vivado program provided. The usable FPGA pins that can be used are routed to two FMC-HPC[15] connectors.

A total of 138 differential pins (or 276 single-ended) grouped into differnet IO-banks of the FPGA pins can be used. The pin assignment is shown in table C.1, C.2 and C.3, where it is also shown which IO bank the pins belong to. Care has taken, that the high frequency ADC outputs are on the same IO-bank for each individual ADC, so that a fast, simultaneous readout can be guaranteed. All outputs of the FPGA are limited to a 1.8 V logic signal standard. The differential inputs are capable of an up to 2.5 V logic standards. As the ADC provides 2.5 V differential signals (LVDS), those can be directly connected to the FPGA. Additionally, the FPGA is equipped with 37 Mb of block RAM and a 1 GB DDR3 RAM.

[15] An FPGA Mezzanine Card connector in the high pin count version with 400 pins, from which 160 pins can be used as signal pins.

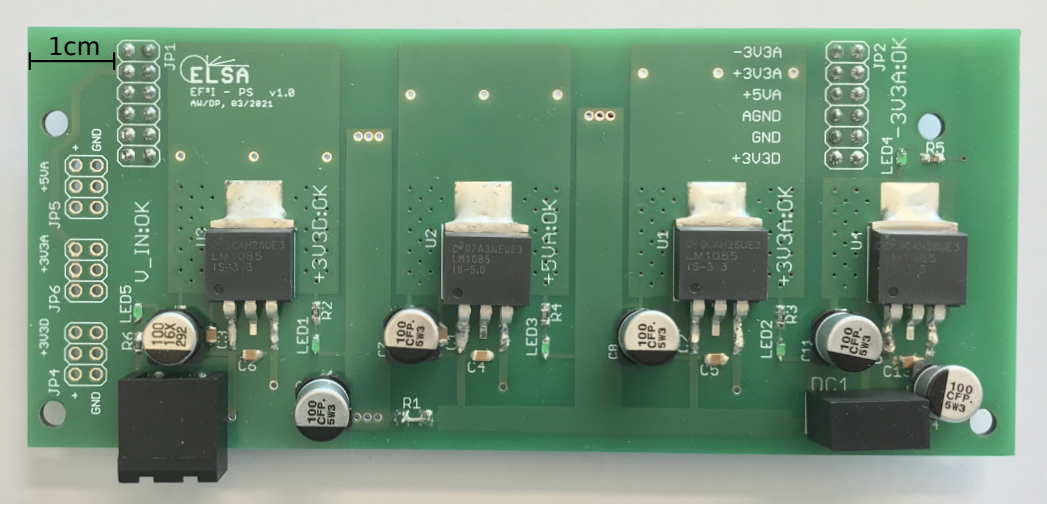


Figure 4.13: Photo of the top side of the Power Supply board

4.3.2 FPGA Configuration

The configuration of the FPGA can be divided into four different sections:

- ADC readout
- Global clocking
- Intermediate data storage
- Data transmission

An overview block diagram is shown in figure 4.14. This section only contains a basic overview on the FPGA configuration. Therefore, giving the HDL code is out of scope for this document[16].

ADC readout Each of the four ADCs provides 12bit of LVDS outputs for the data (DATA), one bit LVDS output for an overrange indicator (OVR), which indicates if the signal to be sampled is outside the input range of the ADC. In addition, there is a data ready signal (DRY), which is provided as one bit LVDS. The data outputs and the OVR signal are synchronous to the DRY signal (see timing diagram in figure 4.15), which has half the sampling frequency (250 MHz) and their phases are shifted.

In the block diagram in figure 4.14 it is shown, that the DATA, the OVR and the DRY signal are routed to one IO-bank for each ADC (see C.1). For each data outputs, which provide the data synchronous to the positive edge and the negative edge of the corresponding DRY signal. The data is read into the FPGA with the help of a double data rate (DDR) input buffer. The DRY signal corresponding to the data is used as the clock for reading procedure. The inputs are delayed using the FPGA build-in primitives, so that the data input latching of the DDR takes place, when all input signals are settled (see timing diagram in figure 4.15). An incorrectly selected delay is characterized by at least one bit having a fluctuation. Especially, with more significant bits, this can be recognized

[16] Available via internal git repository

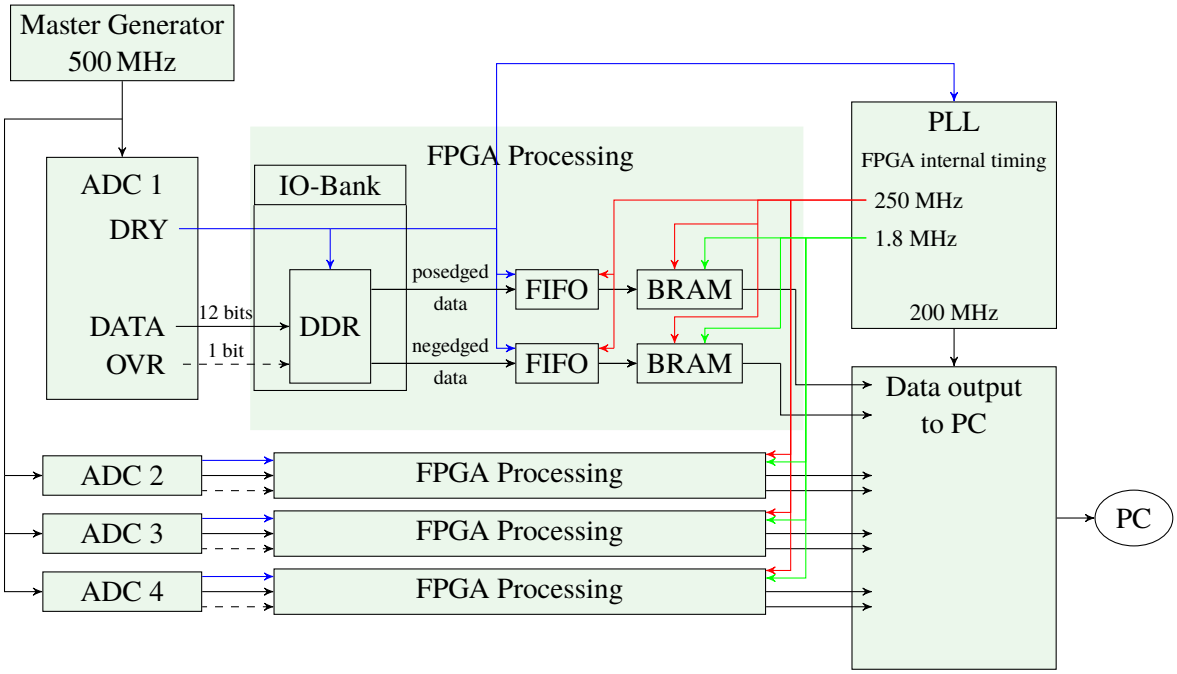


Figure 4.14: Block diagram overview of the FPGA configuration

very well, because the sampled value does not fit to the others. If the inverted logic value is taken for the incorrectly evaluated bit (i.e. instead of a 0 a 1 and vice versa), the sample value fits again into the measurement series. This can also happen with several bits at the same time, which can be noticed in a seemingly random distribution of the sampled data. This is not a sampling problem of the ADC, but a read-in problem of the FPGA. The calibration of the built-in delays was done manually by switches included on the board during calibration in the lab.

The data is output from the module on two signal paths (so called wire) each, one providing the data from the positive edge and one providing the data from the negative edge. The output data of the module is still synchronous with the corresponding DRY signal but has single data rate.

Global clocking of the FPGA The FPGA is internally clocked mainly at 250 MHz. This clock is derived from the DRY signal from one ADC, which is stabilised with a PLL (see figure 4.3.2). Since the frequency of the DRY signals of the four ADCs correspond exactly to half of the sampling clock of 500 MHz, the frequencies of all DRY signals are equal, but they are out of phase. It follows that the FPGA internal 250 MHz clock has the same frequency as all four ADCs DRY signals.

To enable further processing of the output data signals of the DDR modules, which are synchronous to the corresponding DRY signal, two FIFOs for each DDR module are used to cross the clock domain to the internal 250 MHz clock of the FPGA. This means that all data can be processed in parallel with the same clock.

From the clock stabilized by the PLL, additionally a 200 MHz clock is derived, which is needed for internal logic, e.g. for the data transmission stage. In addition, a revolution clock is derived, which is synchronous to the revolution frequency of one bunch. The revolution frequency is obtained by dividing the frequency of the master generator (500 MHz) by the number of bunches in the Stretcher

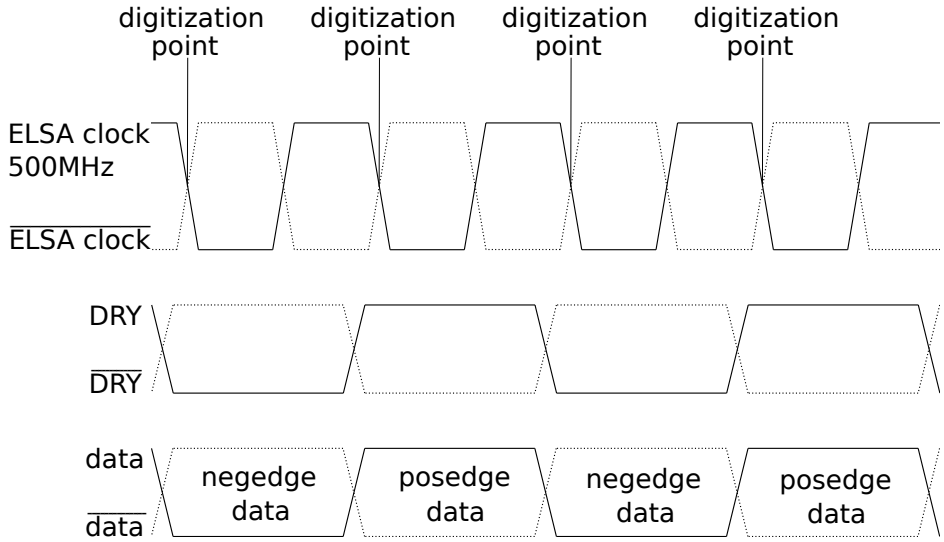


Figure 4.15: Timing diagram of the ELSA 500 MHz sampling clock and the corresponding ADC output signals.

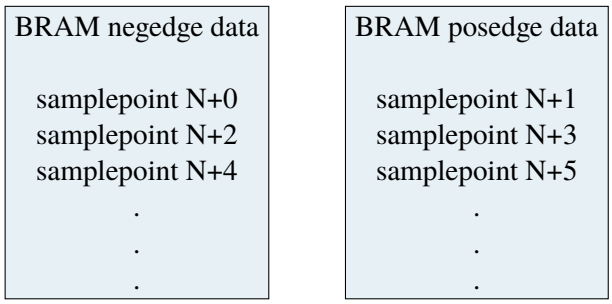


Figure 4.16: The posedge data is stored in one block ram, the negedge data in another. This means that the digitized sample points are alternately stored in the two BRAMs.

ring (274). This gives a frequency of 1.8 MHz which is achieved in the FPGA by dividing the 250 MHz clock by half the bunches (137). At the moment, the revolution clock is used to enable a designation of the bunches during several successive measurements. This is only necessary until the system is integrated into the ELSA timing system, where a revolution clock is available.

Intermediate Data Storage The data outputs, which were routed through a FIFO to switch the clock domain to the internal clock of the FPGA, are stored in Block RAMs (BRAMs), which read and write the data synchronous to the 250 MHz clock. The storage is always started with the same bunch, i.e. synchronously with the revolution clock. This allows repeatable measurements. The problem with this solution is that the revolution clock is no longer synchronous to the same bunch, when the PLL loses its lock or the assignment is irrevocably lost, after a power cycle, resulting in an unclear bunch assignment in reference to the timing system. Therefore, integration into the timing system is indispensable.

The BRAM is 12 bits wide, to enable the data stored in fill resolution. The posedge data and the negedge data are first written separately to two BRAMs, as shown in figure 4.16.

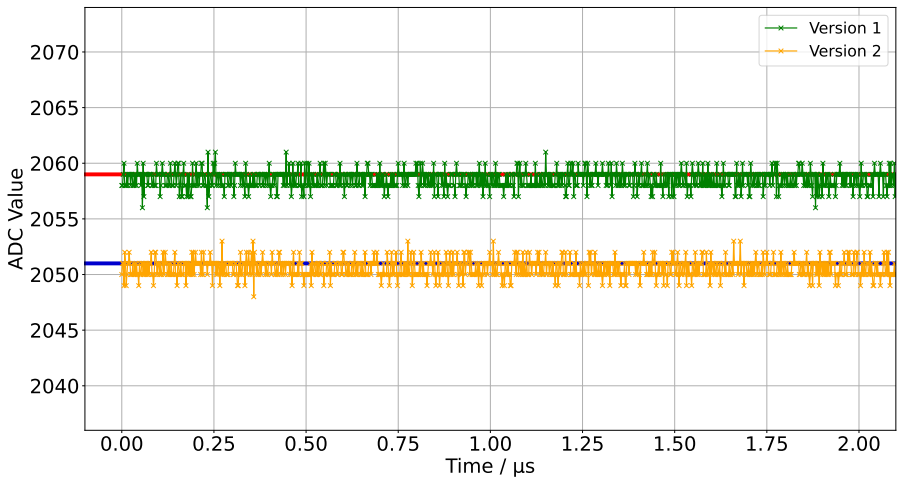


Figure 4.17: Base lines of both versions of the Digitization boards

One block of Ram has a depth of 1024, so 1024 sampling points from the ADC can be stored per BRAM. To be able to store more, 8 BRAMs per ADC were connected in series for the posedge data and 8 for the negedge data. This means that a total of $1024 \cdot 8 \cdot 2 = 16,384$ sampling points can be stored until all BRAMs are full and the data transmission starts. This means that contiguous data can be taken over nearly 60 revolutions of the beam

Data transmission Unfortunately, a data transmission via ethernet in quasi real time was not achievable within the time constraints of the thesis. Therefore, only a slower data transmission via serial UART interface was implemented. For more information on data transmission, see Appendix D.

4.4 Evaluation of the Digitization Boards and the FPGA Configuration

In order to test the Digitization boards and to verify the correctness of the FPGA Configuration, the Digitization boards were tested out in the laboratory. The measurements were performed for both versions of the Digitization board. To create conditions that are as realistic as possible, a 500 MHz sinusoidal signal from a frequency generator was provided as sampling clock for the ADC on the Digitization boards. A sampling frequency of 500 MHz leads to a sampling point every 2 ns. The Digitization boards are connected to the FPGA via the FMC-ADC adapter provided for this purpose. As described in section 4.3.2, the ADC data is read from the FPGA, buffered and sent to a PC for final storage. The FPGA program was equipped with twice as many BlockRAMs for the evaluation of the Digitization board, so that $1024 \cdot 16 \cdot 2 = 32,768$ contiguous data points can be taken per measurement series.

First no input signal was selected, so that the two ADCs each record their specific base line. The raw data output from the ADC, which will be called *ADC value* in the following, is plotted in figure 4.17. The red and the blue lines in the plot show the mean value of all sampling points for the respective ADC. Since the ADC has a 12 bit resolution and the analog differential voltage input range is 2 V_{pp},

Version	1	2
Mean	2059	2051
Standard Deviation	1	1
Highest measured value	2061	2054
Lowest measured value	2056	2048
Maximum absolute deviation	3	3

Table 4.1: Results of the zero measurements shown in figure 4.17. All values are given in units of *ADC value*.

the signal therefore oscillates around 0 (for more information see [18]). Thus, the expected zero point in units of *ADC value* is $2^{12}/2 = 2048$. The measurement evaluation is shown in table 4.1. It can be seen that the base lines for the two boards are individually shifted towards the zero point, but that there is almost no fluctuation around it. Furthermore, it can be seen that the absolute deviation from the mean in both cases is 3 in units of *ADC value*. This corresponds to an absolute fluctuation, given as 6 in units of *ADC value*, of the last 3 bits of the respective ADC.

The next step is to measure the digitization of an oscillating signal in order to evaluate the digitization of varying values on the one hand and the analog input bandwidth of the board on the other hand. Since a continuous measurement series is 64 µs long, at first, care must be taken that the signal to be sampled undergoes at least one oscillation during this time so that the *ADC value* changes during the measurement and the measured function can be evaluated. This corresponds to a minimum frequency of $1/64\,\mu s = 15.6\,kHz$. Second, according to the theorem of Nyquist-Shannon, the frequency to be sampled must not be greater than at most half the sampling frequency, which in this case is 250 MHz. A sine of this frequency could not be evaluated by eye as a first evaluation, but this would be useful for a first test. In addition, one would have exactly one sampling point per half-wave, which makes an evaluation with regard to fluctuations in the digitization process difficult or impossible. Therefore, a substantially smaller frequency in the range of 100-1 000 kHz should be chosen. Sampling of frequencies in this range is not possible, due to an input capacitor, which is necessary for the differentiation of the single ended signal, acts as a high pass. Moreover, as input frequencies of at least 500 MHz are expected for the later application, a correspondingly high bandwidth should be tested. Therefore, an input frequency of 499.669 MHz was chosen to evaluate a input bandwidth of ~500 MHz, but the sampled signal is an undersampling artefact due to aliasing, because the 500 MHz sampling frequency is less than twice of the input frequency. Therefore, only the difference between the two frequencies, which is 331 kHz, can be derived from the sampling points. The measurement idea is illustrated by a principle sketch in figure 4.18. Here, a larger frequency difference between sampling frequencies (500 MHz) and input frequencies (in this case 400 MHz) was chosen to illustrate this more clearly. One can see that the resulting frequency of 100 MHz is exactly the difference between sampling and input frequency.

The measurement was repeated at twice the input frequency, i.e. 993.338 MHz. Here, the input bandwidth is increased to ~1 GHz and the difference between input and sampling frequency is doubled to 662 kHz. The corresponding measurement series are shown in Figure 4.19, together with the baseline for the ADC on Digitization board version 2. Both measurement series were fitted with a sine function,

$$f(x) = a \cdot \sin(b \cdot x + c) + a_{\text{harm}} \cdot \sin\left(2 \cdot b \cdot x + c_{\text{harm}}\right) + d \tag{4.1}$$

which also includes the first harmonic. For example, a frequency generator always produces parts of a

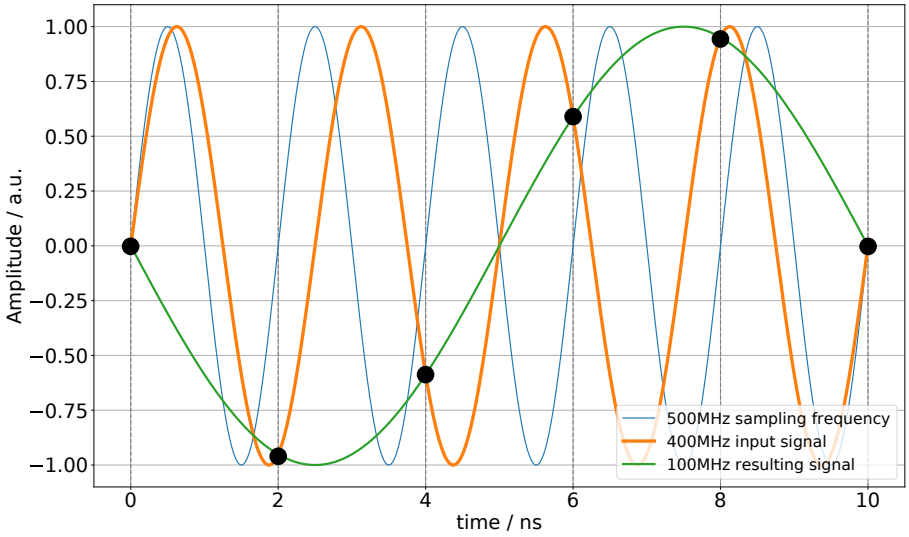


Figure 4.18: The sampling frequency is shown in blue, where the actual sampling times are shown with a dashed grey line, whereby the sampled value at this time is marked with a black dot. The input signal is drawn in orange and the resulting signal in green.

Parameter	499.669 MHz	999.338 MHz
a / *ADC value*	976.11 ± 0.01	712.67 ± 0.02
b / kHz	330.520 ± 0.002	661.043 ± 0.002
c	4.83621 ± 0.00003	4.83621 ± 0.00003
a_{harm}/ *ADC value*	5.64 ± 0.02	3.00 ± 0.02
c_{harm}	7.677 ± 0.003	6.118 ± 0.007
d / *ADC value*	2050.53 ± 0.01	2051.23 ± 0.01

Table 4.2: Fitted parameter of function 4.1.

harmonic, so it is not unexpected that there is a harmonic contribution as well.

The parameters, obtained by a fit with the program gnuplot[17], are listed in table 4.2. The fundamental frequencies are as expected 331 kHz and 661 kHz. A small inaccuracy may occur due to the frequency generators not producing exactly the desired frequency. The harmonic found has a much smaller amplitude than the fundamental frequency. Unfortunately, a meaningful normalization of the *ADC values* into a voltage is not possible, since the amplitudes of the signals, which are actually of the same size, are attenuated by different amounts, mainly due to frequency-dependent attenuations on the board.

The same measurement was carried out for Digitization board version 1. The results of this can be found in the appendix E. Due to previous tests on Digitization board version 1, which led to a redesign of the board, these measurements and the measurement with version 2 are not directly comparable.

[17] see http://www.gnuplot.info/

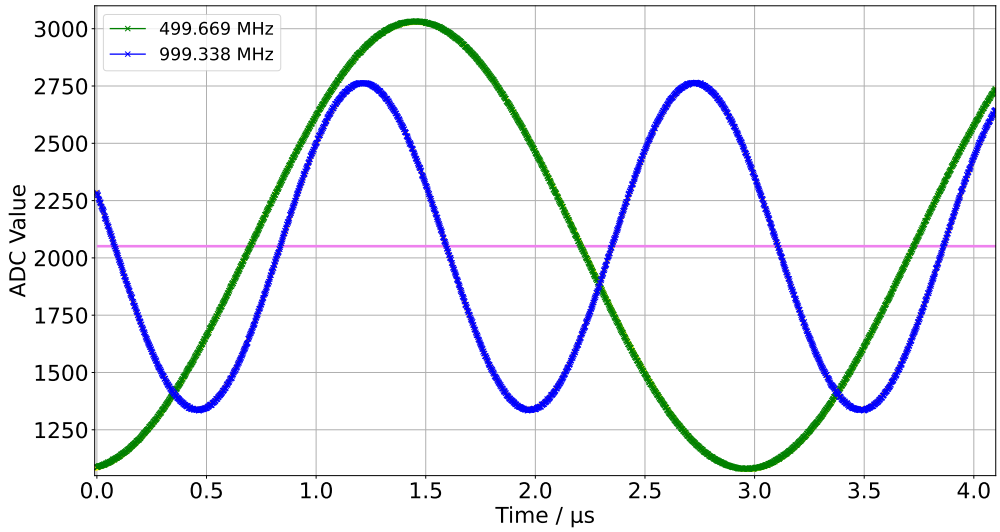


Figure 4.19: Measurement with Digitization board version 2 of a sin of RMS-amplitude 600 mV maximal amplitude with frequency displayed in the plot. The base line, displayed in table 4.1, is drawn in violet.

It could be shown that the FPGA is configured correctly and that a sampling of the frequencies 500 MHz and 1 GHz works as expected.

CHAPTER 5

Measurements at the Stretcher Ring

After the Attenuation and Amplification board (see section 4.2.1) and the Digitization board (see section 4.2.2) were evaluated under laboratory conditions and the FPGA configuration (see section 4.3.2) was also verified under laboratory conditions, a measurement was performed at the Stretcher ring. For the measurement, a proper BPM signal, generated by the electron bunches, is sampled synchronously to the 499.669 MHz master generator signal, which is the acceleration frequency, with which the bunches pass through the BPM.

The measurement setup, which should resemble as closely as possible the future EF^{2}I system will be set up, is sketched in Figure 5.1. The measurement was set up at the DESY BPM, which is located

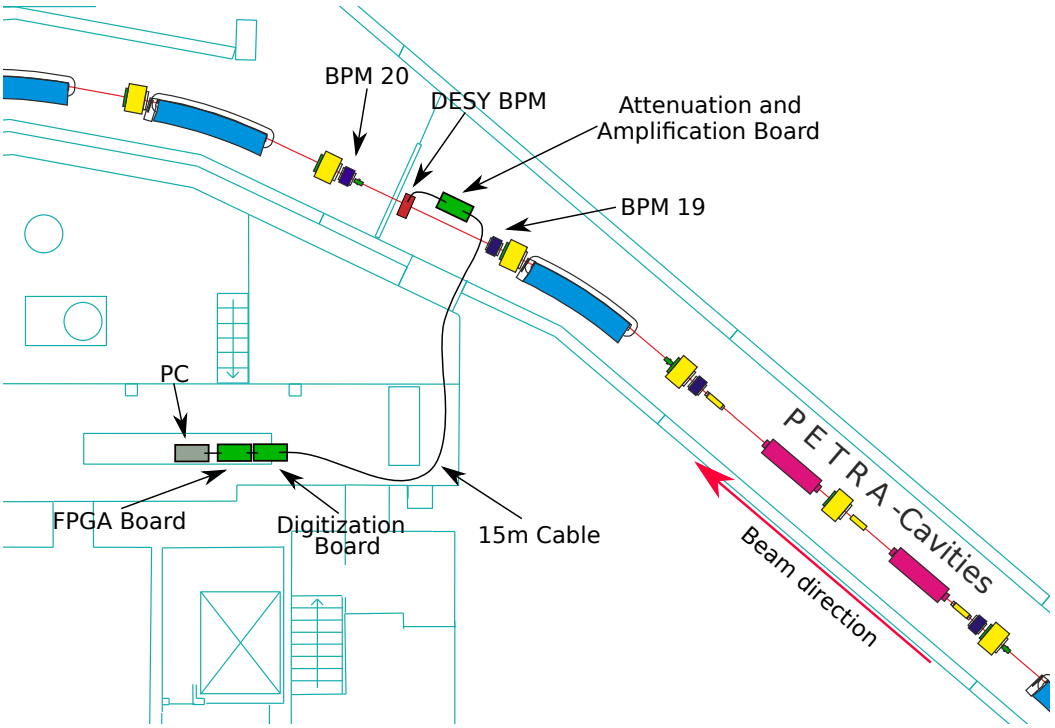


Figure 5.1: Sketch of the Measurement with the EF^{2}I system at the Stretcher ring. In light blue, the building outlines of the Physics Institute are drawn.

in the Stretcher ring in beam direction behind the PETRA-cavities between BPM 19 and 20 of the beam position measurement system. From the BPM pickup electrode 4 (compare figure 2.3) was read out, since only one digitization channel was accomplished at the time of the measurement.

The electrode signal is amplified in the tunnel of the Stretcher ring with the Attenuation and Amplification board, which was configured to the maximum value of 20 dB. For this, electrode 4 and the input of the PCB are connected with a 1 m long 50 Ω coaxial cable[1] with N-type connectors. The amplified signal is provided at the Attenuation and Amplification board at output port 4. From there, it is transmitted with a 15 m long 50 Ω coaxial cable[2] with N-type connectors into the adjacent so-called RF room of the facility. Here, it is used as analog input signal for input port 2 of the Digitization board.

The Digitization board (version 1) receives a differential signal as sampling clock, which is generated by an LVDS compatible comparator using the single-ended signal of the rf master generator, which is also located in this room. The Digitizing board is connected to the FPGA board via one of the FMC-ADC Adapter boards. The FPGA reads the data from the ADC, stores it temporarily and then sends it to the PC, as shown in figure 4.14. The FPGA is configured to take and store 16,384 data points which are then sent to the PC. After that, the sampling, respectively the data storage, starts all over again. As the data acquisition is started synchronous to the revolution clock, it is ensured that the first stored bunch is always the same, so that several data sets can be compared with each other.

For the final EF^{2}I system it is planned that also the Digitization board and the FPGA board are located in the accelerator tunnel, so that less attenuation by cables is to be expected. At the time of measurement, they were not placed in the tunnel, firstly, to avoid exposing the sensitive ICs to ionizing radiation and secondly, to allow working next to the boards. In the final system, a radiation-proof enclosure will be built and the FPGA data will be fed into the ELSA network via ethernet. For the measurement, the accelerator was operated in Syli mode (see 1.4), since here, in contrast to the other modes, there are only small fluctuations in the current and the beam, and thus remains the same over several thousands of revolutions. It operates at a constant electron energy of 1.2 GeV.

To damp horizontal, vertical and longitudinal bunch oscillations (see section 2.1.1 and 2.1.2), the bunch-by-bunch feedback system (see section 2.2.1) is switched on in all three dimensions during the measurement, unless otherwise described (see section 5.2).

Due to a spontaneous upgrade of the beam line, further measurements at ELSA were not possible within this thesis. Since unfortunately only one digitization channel was completed at the time of the measurement, the sampling time adjustment (described in section 3.3) could not be carried out. By operating the accelerator in Syli mode, it could be assumed that no beam loss, bunch oscillation or a change in beam position occurred. Under these constant conditions, the variable delay was set manually to a sampling time, where the measured values were highest. Since this measurement naturally does not guarantee that digitization takes place at the optimal sampling point, an increased influence of the natural jitter must be expected in future measurements taken place at non-ideal conditions.

5.1 Filling Pattern Measurement

The measurement was carried out as described in section 3.3 to determine the filling structure of a homogeneously filled beam and a semi-filled beam. A homogeneous filling pattern is achieved by

[1] Attenuation at 500 MHz is 2.77 dB and at 2.4 GHz it is 5.98 dB

[2] Attenuation at 500 MHz is 0.33 dB and at 2.4 GHz it is 0.98 dB

varying the injection timing with respect to the phase of the revolution frequency of the bunches from the Booster synchrotron into the Stretcher ring, whereas for a semi-filled filling pattern the injection always occurs at the same time (see [9, section 6.5]). For the second case, one expects exactly 116 buckets, i.e. exactly the number of buckets in the Booster synchrotron, to be filled and the rest to be empty. Since the extraction takes a finite time due to finite rising times of the extraction elements in the Booster synchrotron, there will not be a hard jump in the filling pattern, but a slow rise and fall. In figure 5.2, the measured raw output data of the ADC is plotted for each bunch for the two different filling patterns of the beam. The 274 buckets are plotted on the x-axis, whereby the sampled

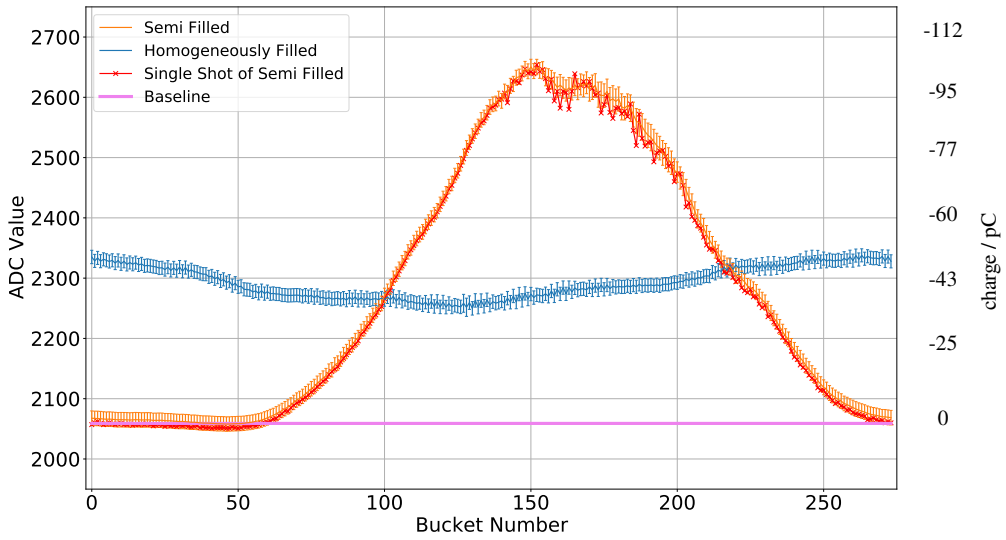


Figure 5.2: This plot shows the mean values of the ADC samplings for each bucket over 2950 revolutions of the electron beam in the Stretcher ring. For the means shown in blue, a homogeneously filled pattern and for the data points in orange a semi filled pattern of the electron beam were produced. The red data points show a single shot of the semi filled pattern of the electron beam during one revolution. The baseline is drawn in violet.

values can be clearly assigned to the bucket number, but the bucket numbering is not connected to that in the accelerator's timing system. The y-axis shows the sampled data values, which are given as raw data in units of *ADC value* on the left side. This is the output value of the ADC, which is between 0 and 4096. The value is proportional to the voltage of the sampled signal, where 2059 (see 4.4) corresponds to a voltage of 0 V. In the plot, this baseline at 2059 is drawn in violet. Since the voltage of the sampled signal is proportional to the charge of the bunch, the ADC value is also proportional to the bunch charge. Therefore, taking into account the shift against the baseline, the y-axis can be converted from *ACD value* to *bunch charge* measured in pC as described in section 3.2.1. The averaged beam current I_{beam} was determined for the homogeneous filling being approximately 20.6 mA and for the inhomogeneous one being approximately 20.5 mA from the control system. This results in a calibration factor k of (-0.176 ± 0.002) pC per *ADC value - baseline*.

For the orange and blue plotted data, sampling points $q_{\mathrm{b},\,i,n}$ over $N = 2950$ revolutions were

collected and averaged, where the mean values and the corresponding RMSE_i[3], given by

$$\mathrm{RMSE}_i = \sqrt{\frac{\sum_{n=0}^{N} \left(q_{\mathrm{b},i,n} - \bar{q}_{\mathrm{b},i}\right)^2}{N}} \tag{5.1}$$

with

$$\bar{q}_{\mathrm{b},i} = \sum_{n=0}^{N} \frac{q_{\mathrm{b},i,n}}{N} \tag{5.2}$$

$$\tag{5.3}$$

for $i \in [1, 274]$, were calculated and plotted. It is noticeable that some of the sampled data points appear to be below baseline, resulting in a positive charge of the bunches, which can not be explained physically. Also noticeable are larger than expected RMSE_i values, which are drawn as error bars around the mean values. One would expect RMSE_i values in the order of ±3 in units of *ADC value* (see 4.4). The mean of all RMSE_i values is 11 for the measurement of the homogeneous filling pattern and 13 for the semi-homogeneous one. To explain this fact, figure 5.3 shows the mean over all 274 buckets per beam revolution plotted for each revolution for the semi filled electron beam. In addition, the individual values of three selected bunches

- Bunch 149, a strongly charged bunch
- Bunch 223, a bunch on the falling slope
- Bunch 40, an uncharged bunch, i.e. a quasi-empty bucket

for each revolution are plotted for the same data set. The baseline is given in violet. In the ideal case, one would expect the mean value to be constant per revolution or that it would decrease steadily when there is a loss of current in the accelerator. This ideal case cannot be recognized in the plot On the contrary, the mean value fluctuates. The mean values are determined to be 2289 ± 12 for the mean (blue data points), 2640 ± 12 for bunch 149 (orange data points), 2320 ± 12 for bunch 223 (purple data points) and 2061 ± 11 for bunch 40 (green data points). It is striking that the signal of all bunches and the mean perform a very similar oscillation. Moreover, even for the actually uncharged bunch 40 this oscillation is present around the baseline, and thus seems to have alternately a negative as well as positive charge. The measurement thus clearly shows that there is a background oscillation on the signal to be sampled. Therefore, at this stage, it is not yet useful to determine a global calibration factor, as in section 3.2.1. The converted axis labeling serves in this case only as an estimate of the quantities.

Due to a storage programming mistake in the FPGA configuration, exactly 16 values per 59 revolutions, which corresponds to the first value of the 16 BRAMs used in each case, are unusable and were therefore not taken into account in the evaluation. For more information see F.

The measurement showed that a filling pattern analysis of the beam can be done with the new system. It is assumed that the main reason for this background oscillation is an oscillating reference potential difference between electrode signal and clocking signal. This will be eliminated, when the

[3] short for *root-mean-squared-error*

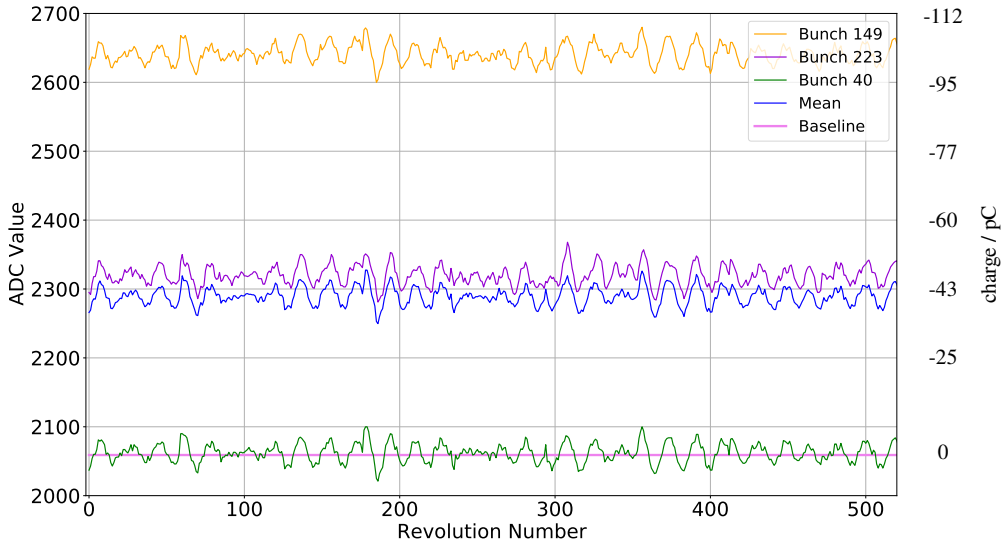


Figure 5.3: The mean of the ADC values of all bunches of the electron beam and the ADC value of three single bunches is plotted against the number of revolutions.

entire measurement setup is set up in the accelerator tunnel. Because of this background oscillation, a more precise calibration of the charges is not yet possible.

5.2 Longitudinal Oscillation Measurement

As explained in section 2.1.1, the bunches may perform an oscillation in longitudinal direction. This oscillation is suppressed by the bunch-by-bunch feedback system, but its amplitude will never decrease to zero. If the feedback system is switched off in longitudinal direction, the oscillation is not suppressed anymore. This leads to a temporal oscillation of the arrival time of the bunches at the BPM and thus an amplitude oscillation induced signals on the electrode, which is sketched in figure 5.4. The "sampling point" is the time of sampling of the induced electrode signal. The induced signal from an oscillating bunch, where the maximum time variation is shown in blue compared to the non-oscillating ideal position in red, causes a shift of the maximum of the amplitude compared to the sampling point. Therefore, the sampled points will oscillate around the value of the center position. In the figure 5.4, it can also be seen that a forward shifted bunch will have a smaller sampled amplitude than a backward shifted one. This follows from the asymmetry of the induced signal around its first maximum. This difference is not very large in the range of an expected oscillation, so that a sinusoidal oscillation of the sampled values can be expected, whereby also shares of the higher harmonics will be present. This sinusoidal oscillation should have the same frequency as the oscillation of the bunches. Therefore, the frequency should be equal to the synchrotron frequency.

To measure the synchrotron frequency, the accelerator was semi-filled, as already shown in figure 5.2. After a measurement was made with the longitudinal feedback system switched on, where the

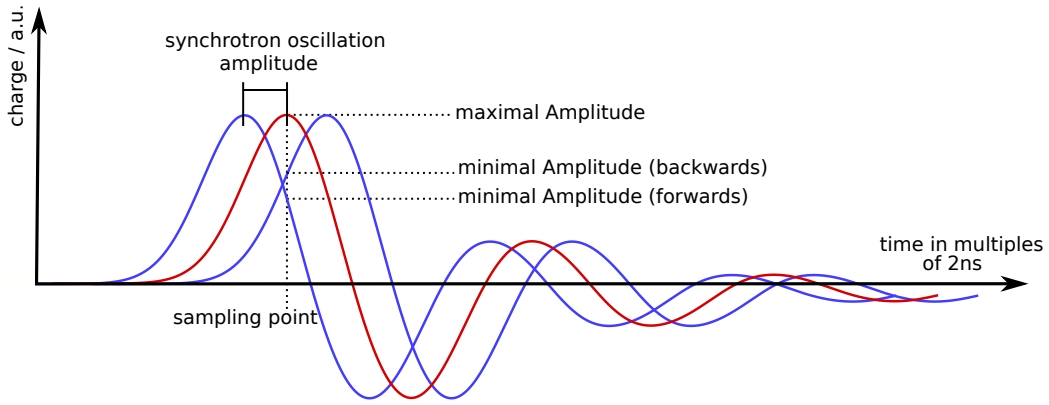


Figure 5.4: Sketch of induced bunch signals, where the bunches oscillate longitudinally, thus the signals does. Not to scale.

oscillation was damped, a second measurement was conducted with the feedback system was switched off, enabling the oscillations to arise. Both measurements were Fourier transformed to look at the individual frequency components. The results are shown in Figure 5.5. For the blue data series, the

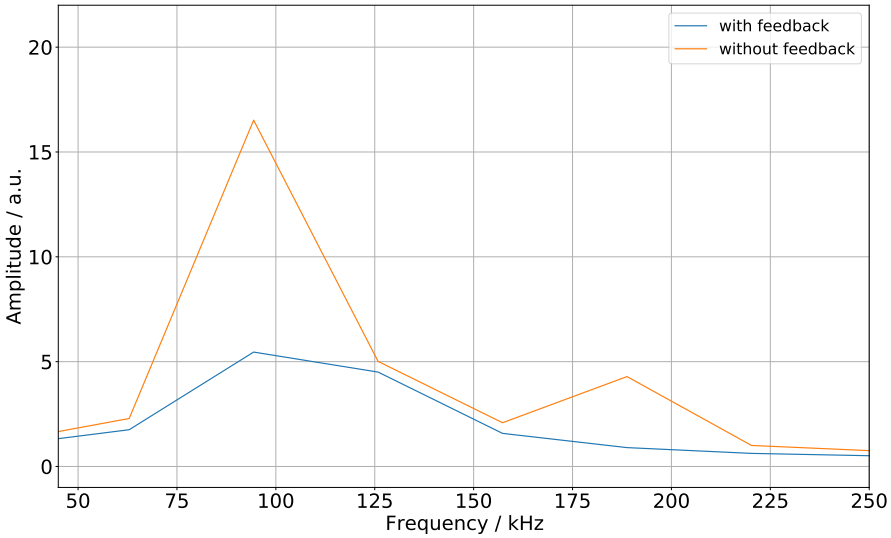


Figure 5.5: Longitudinal bunch oscillation due to synchrotron oscillation.

feedback system was switched on in all three directions. For the orange data series the longitudinal feedback system was switched off. Unfortunately, too few contiguous data points were taken during this measurement for a higher frequency resolution. Additionally, the measurement could not be repeated due to the beamline upgrade.

By comparing the two Fourier transforms, it can be seen that in the measurement series for the switched-off feedback system an amplitude increase at approximately 90 kHz and also at 180 kHz

becomes visible. For both measurements, the synchrotron frequency was set to 89 kHz, indicating that the amplitude increase in this frequency range is exactly the synchrotron frequency and its first harmonic. As more contiguous sampling points are taken, the frequency resolution of the Fourier transform will improve. This will be possible with the new configuration with extended memory in the FPGA.

This measurement can also be applied to horizontal and vertical oscillations, enabling the measurement of the tune in these planes. However, this is only possible with all four digitization channels, so that a position measurement can be carried out.

5.3 Verification of a Single Bunch Resolution

With the new EF^{2}I system, it should be possible to measure the charge of individual bunches without the influence of the neighbouring bunches. This influence could emerge, for example, due to a too small analogue input bandwidth or due to overlapping signals. To verify a single-bunch resolution, one can create a filling pattern with bunches, which are differently charged, next to each other. This is given with a filling pattern, in that every second bunch was cleared by occasionally exciting certain a multi-bunch mode. This could be verified very well, as a multi-bunch mode was excited in an already filled beam, whereupon the charge of every second bunch was minimized. More information about multi-bunch modes can be found in [28, chapter 8].

The measurement was performed exactly as described in section 5.1 and the corresponding results of filling pattern are shown in figure 5.6. For the plot, the average value over the sampled amplitudes

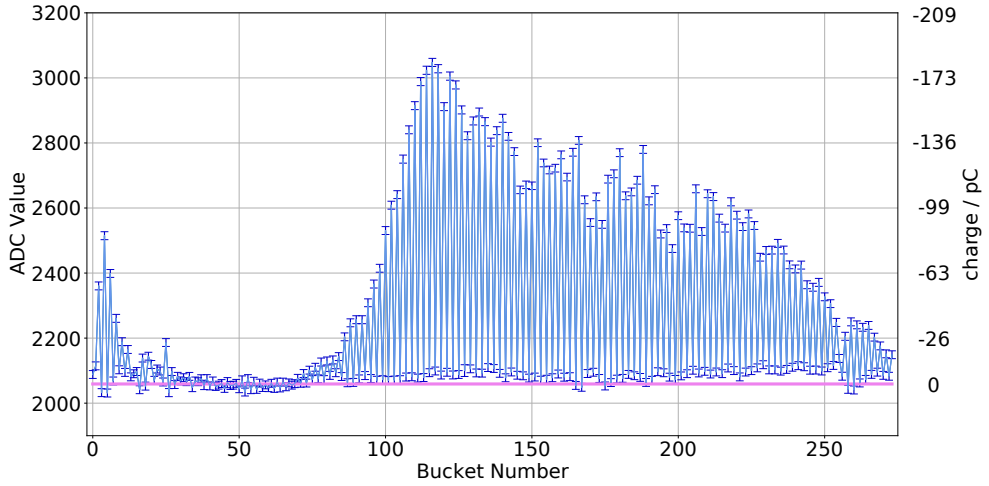


Figure 5.6: The mean values of the ADC samplings for each bunch over 2950 revolutions is shown, whereby a multi-bunch oscillation was excited, so that every second bunch has left the electron beam.

of the respective beam signal of 2950 beam revolutions was calculated and plotted. The baseline is again plotted in violet and the y axis is transformed from units of *ADC value* to *picocoulomb* as explained above. The mean beam current was determined from the control system to be 18.5 mC, resulting in a calibration factor k of approximately -0.184 pC per *ADC value - baseline*. The RMSE

(according to equation 5.1) is plotted as error bars. The mean of the RSME values is 12 in terms of *ADC value*. This is in the same order of magnitude as the scatter of the sampling points from the measurement of the homogeneous filling structure, as well as the semi-filled. The fluctuation of the measured values can again be explained by a background oscillation on the signal.

This measurement leads to the conclusion, that a single bunch resolution is possible with the EF^2I readout system for measuring the bunch charges.

5.4 Bunch Cleaning with the Bunch-by-Bunch Feedback System

The bunch-by-bunch feedback system (see section 2.2.1 and for more information [28, chapter 6]) can be used to excite coherent betatron oscillations of the individual bunches until they leave the acceptance range of accelerator and are lost. With this technique arbitrary filling patterns can be generated. With the EF^2I system, an evaluation of this bunch bleaning procedure is possible. For this purpose, all buckets are first filled homogeneously. From this starting pattern, several bunch sequences in groups of 10 bunches are excited simultaneously.

The results of the measurements are shown in the figure 5.7. All three data point sets are acquired

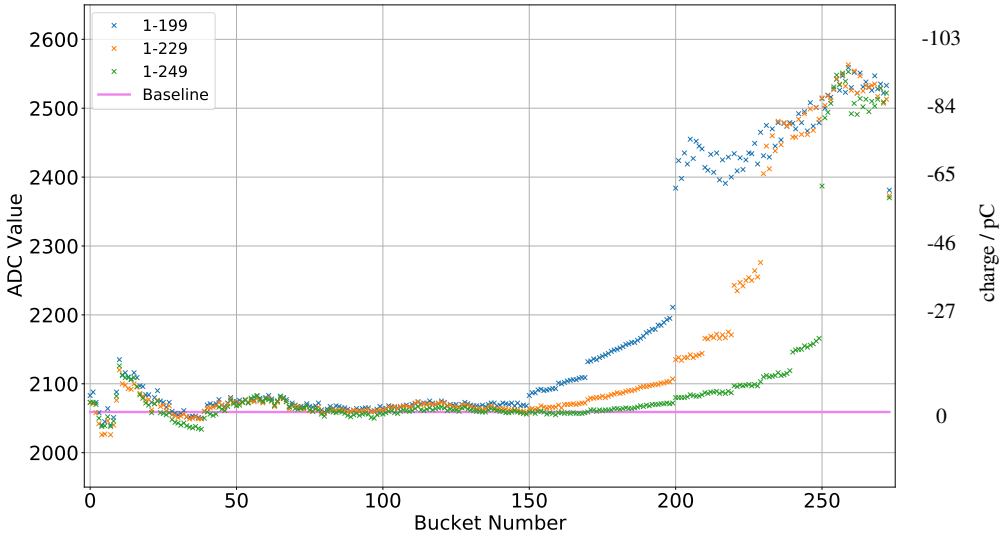


Figure 5.7: The filling pattern of the electron is shown for one revolution of the electron beam, with different sequences of bunches being excited with the bunch-by-bunch feedback system, so that the electrons are partially or completely removed from the beam, for the different measurement series.

using only one revolution of the beam without averaging. Furthermore, the baseline is drawn in violet. The calibration factor was calculated to be (-0.19 ± 0.02) pC per *ADC value - baseline*, due to the mean beam current of 11.7 mA, resp. 8.5 mA, resp. 5.2 mA. From the initially homogeneously filled beam, the bunches up to approximately bucket number 150 were cleared out first. About these only the statement can be made that there are no or hardly any electrons left in the buckets.

Therefore, the interesting section of the plot between bucket 150 and bucket 274 has been plotted as a detail view in figure 5.8. From here on, the grey dashed vertical lines indicate jumps between the

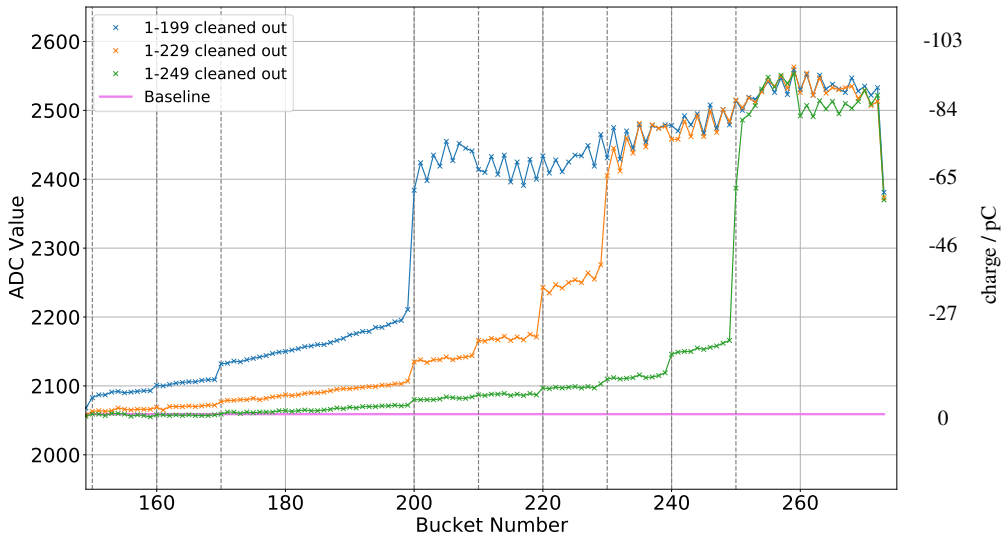


Figure 5.8: Enlarged section from figure 5.7

charges of neighbouring bunches. The bunches were always excited simultaneously in sequences of 10 each. Apparently, these jumps occur in all three measurement series at the same bucket number. This indicated that the bunch cleaning does not works perfectly and leaved a residual charge in every bucket. With further excitement of adjacent bunches, the residual charge shrinks in these buckets as well.

It is also noticeable that bunch 274, which should have not been excited is less charged as the other non excited bunches. In this case, the impact of the bunch cleaning on neighbouring bunches can be seen in this steep slope (compare to [28, figure 10.2]).

With the EF^{2}I readout system, the operation of the bunch cleaning of the bunch-by-bunch feedback system could be analysed and its single bunch resolution could be verified.

CHAPTER 6

Summary and Outlook

The aim of this master thesis was to design and build a fast readout system for a BPM already installed in the beam pipe of the ELSA Stretcher ring. With an already existing readout system only a position measurement, which is averaged over all 274 bunches and additionally over 2000 revolutions, is possible. The new readout system enables a determination of the absolute charge for each individual bunch and for each individual revolution in order to derive the filling pattern of the electron beam. In addition, the system should allow an position measurement with single bunch resolution. in order to derive the filling pattern of the electron beam.

To achieve this, the EF^2I readout system was developed and a first version was already tested in the Stretcher ring. It could be verified, that the PCBs and the FPGA configuration of the readout system were working properly. Since only one digitization channel was completed at the time of the measurement, only the charge measurement could be tested so far, but no position measurement yet. During these tests, performed under nominal operation conditions in the Stretcher ring, a charge measurement was successfully carried out with single-bunch resolution with the EF^2I readout system. In addition, a transformation from the measured relative bunch charges in units of *ADC value* to absolute bunch charges in units of Coulomb is possible.

It is planned to install the remaining 4 channels so that a position measurement for each individual bunch will be possible. The design and production of the PCBs are all finished and most of them have already been tested under laboratory conditions. At the time of the measurement at the accelerator, the voltage supply was ensured with several laboratory power supplies. These have already been replaced by a dedicated power supply board.

Since the charge measurement with one channel allows a single-bunch resolution, this will also be the case for all four channels. The FPGA has essentially already been reconfigured to operate with four channels without further problems. The already tested synchrotron frequency measurement also will have a higher frequency resolution with more sampling points of an individual bunch in contiguous revolutions. In addition, a horizontal and vertical tune measurement will also be possible for a single bunch as soon as the position measurement is in operation. The optimal sampling time of the bunch signal has been set by hand until now, but in the future these timing adjustments will be automated using the concept described in section 3.3. After the beam line upgrade these new featured will be tested and set into nominal operation.

The whole readout system will be installed in the accelerator tunnel next to the BPM, to minimize attenuation of the electrode signals by connection cables. Thus, a larger ADC input range can be

used, resulting in a more precise charge resolution. Having both, input signal and clocking signal, in reference to the same potential, the background oscillations are avoided.

In addition, EF^2I will be integrated into the accelerator-internal control system, so that the data can be displayed and processed in quasi real time. Then the measured filling pattern can directly be compared with, for example, the output data of the bunch-by-bunch feedback system, due to a synchronized bucket numbering.

Once everything will be set up, the calibration parameters for the absolute charge measurement can be calculated using the Syli mode for different beam currents and energies. This stored calibration data enables a fast absolute charge measurement for the individual bunches in the booster mode.

Furthermore, a bunch measurement at the Booster synchrotron, in which also a BPM is installed, can be considered. Its electrode signal has already been evaluated with an oscilloscope. Using the same acceleration process, a measurement at the Booster synchrotron could be possible at least close to the extraction energy of 1.2 GeV and may provide diagnostic capabilities for optimizing the acceleration in Booster synchrotron and the extraction to ELSA.

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APPENDIX A

Testing board

side	track number	track width / μm	Characteristics
top	1	234.6	ground vias next to the track
	2	234.6	with a 0805 0 Ω resistor
	3	234.6	with a 0402 0 Ω resistor
	4	222.0	
	5	210.0	
	6	234.6	90 degrees corners
	7	234.6	135 degrees corners
	8	234.6	bending radius: 9.5 mm
bottom	1	234.6	with a 0603 0 Ω resistor
	2	234.6	
	3	245.0	
	4	200.0	
	5	234.6	rounded corners
	6	234.6	bending radius: 4.5 mm

Table A.1: Different characteristics for the tracks on the testing board. The copper track has a height of 35 µm in each case. The layer configuration 'Definierter Lagenaufbau' (eng.: defined layer structure), described at the website of Multi CB [29], was chosen.

Track analysis of the testing board (see figure 4.2 and table A.1) with a VNA. The measurement setup is sketched in figure (see 4.3). Comparing top4, top5, bottom2, bottom3, bottom4, which have different track widths and top1, which has ground vias next to the track, it cannot be said which of these tracks has an impedance of 50 Ω, because of the relative nature of the measurement. The corresponding plots are shown in figure A.1. A track width of 230 µm was chosen for single ended high frequency signals. For differential signals a track width of 134 µm and a track distance of 125 µm was chosen from the impedance calculator [19] without testing.

For top8 and bottom6, which have different bending radii, the knowledge is that a larger radius is better. The corresponding plots are shown in figure A.2.

From the tracks top6, top7 and bottom8, which have different edges in the track, it can be said, that the impact is not huge. In the plot, which is shown in figure A.3, no significant differences can be

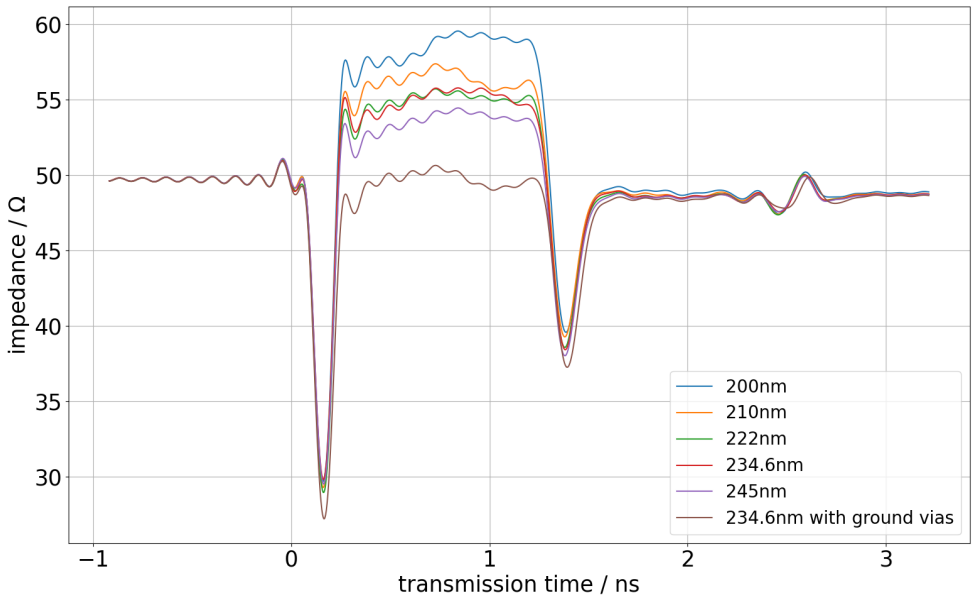

Figure A.1: TDR measurement of different track widths on the testing board. The track of the data plotted in brown has the same width as the track of the data plotted in red but with grounded vias next to it.

seen.

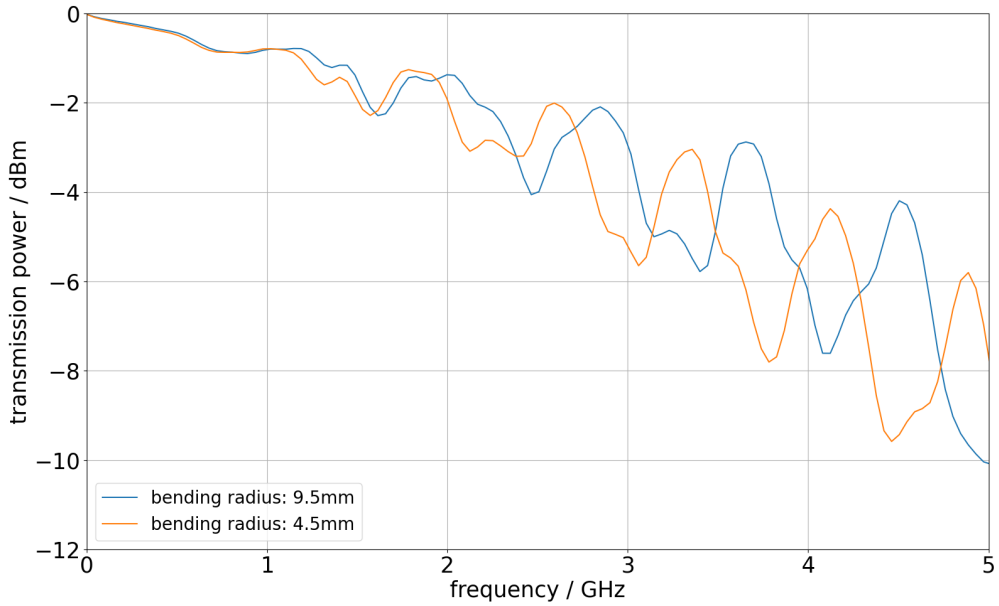

Figure A.2: Comparing two U-turns with different radii of a track on a PCB.

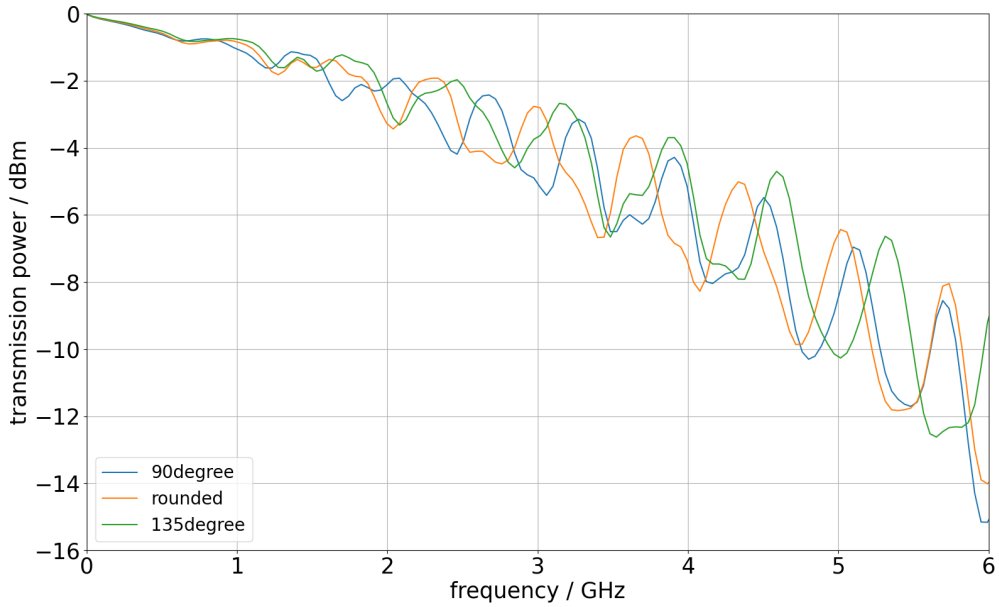

Figure A.3: Comparing different geometries for corners in the conductive track.

APPENDIX B

Digitization Board

Figure B.1: Photo of the first version of the Digitization board.

APPENDIX C

FPGA Pin Assignment

ADC Pin Assignment

ADC0 / ADC2

					FPGA (FMC1)		FPGA (FMC2)	
LOC	**Signal ADC-FMC**	**Pin ADC**	**Signalname FMC-HPC**	**Pin FMC**	**Pin**	**Bank**	**Pin**	**Bank**
ADC	OVR_P	ADC0/2_98	FMCn_HPC_LA15_P	H19	M36	19	AC38	17
ADC	OVR_N	ADC0/2_97	FMCn_HPC_LA15_N	H20	L37	19	AC39	17
ADC	DATA0_P	ADC0/2_94	FMCn_HPC_LA16_P	G18	K37	19	AJ40	17
ADC	DATA0_N	ADC0/2_93	FMCn_HPC_LA16_N	G19	K38	19	AJ41	17
ADC	DATA1_P	ADC0/2_90	FMCn_HPC_LA14_P	C18	N39	19	AB38	17
ADC	DATA1_N	ADC0/2_89	FMCn_HPC_LA14_N	C19	N40	19	AB39	17
ADC	DATA2_P	ADC0/2_86	FMCn_HPC_LA13_P	D17	H39	19	W40	17
ADC	DATA2_N	ADC0/2_85	FMCn_HPC_LA13_N	D18	G39	19	Y40	17
ADC	DATA3_P	ADC0/2_82	FMCn_HPC_LA11_P	H16	F40	19	Y42	17
ADC	DATA3_N	ADC0/2_81	FMCn_HPC_LA11_N	H17	F41	19	AA42	17
ADC	DATA4_P	ADC0/2_78	FMCn_HPC_LA12_P	G15	R40	19	Y39	17
ADC	DATA4_N	ADC0/2_77	FMCn_HPC_LA12_N	G16	P40	19	AA39	17
ADC	DATA5_P	ADC0/2_74	FMCn_HPC_LA10_P	C14	N38	19	AB41	17
ADC	DATA5_N	ADC0/2_73	FMCn_HPC_LA10_N	C15	M39	19	AB42	17
ADC	DATA6_P	ADC0/2_70	FMCn_HPC_LA07_P	H13	G41	19	AC40	17
ADC	DATA6_N	ADC0/2_69	FMCn_HPC_LA07_N	H14	G42	19	AC41	17
ADC	DATA7_P	ADC0/2_66	FMCn_HPC_LA09_P	D14	R42	19	AJ38	17
ADC	DATA7_N	ADC0/2_65	FMCn_HPC_LA09_N	D15	P42	19	AK38	17
ADC	DATA8_P	ADC0/2_62	FMCn_HPC_LA05_P	D11	M41	19	AF42	17
ADC	DATA8_N	ADC0/2_61	FMCn_HPC_LA05_N	D12	L41	19	AG42	17
ADC	DATA9_P	ADC0/2_58	FMCn_HPC_LA04_P	H10	H40	19	AL41	17
ADC	DATA9_N	ADC0/2_57	FMCn_HPC_LA04_N	H11	H41	19	AL42	17
ADC	DATA10_P	ADC0/2_54	FMCn_HPC_LA03_P	G9	M42	19	AJ42	17
ADC	DATA10_N	ADC0/2_53	FMCn_HPC_LA03_N	G10	L42	19	AK42	17
ADC	DATA11_P	ADC0/2_50	FMCn_HPC_LA06_P	C10	K42	19	AD38	17
ADC	DATA11_N	ADC0/2_49	FMCn_HPC_LA06_N	C11	J42	19	AE38	17
ADC	DRY_P	ADC0/2_46	FMCn_HPC_LA01_CC_P	D8	J40	19	AF41	17
ADC	DRY_N	ADC0/2_45	FMCn_HPC_LA01_CC_N	D9	J41	19	AG41	17

ADC1 / ADC3

					FPGA (FMC1)		FPGA (FMC2)	
LOC	**Signalname ADC**	**Pin ADC**	**Signalname FMC-HPC**	**Pin FMC**	**Pin**	**Bank**	**Pin**	**Bank**
ADC	OVR_P	ADC1/3_98	FMCn_HPC_LA33_P	G36	U31	34	T36	18
ADC	OVR_N	ADC1/3_97	FMCn_HPC_LA33_N	G37	T31	34	R37	18
ADC	DATA0_P	ADC1/3_94	FMCn_HPC_LA30_P	H34	V30	34	T32	18
ADC	DATA0_N	ADC1/3_93	FMCn_HPC_LA30_N	H35	V31	34	R32	18
ADC	DATA1_P	ADC1/3_90	FMCn_HPC_LA31_P	G33	M28	34	V39	18
ADC	DATA1_N	ADC1/3_89	FMCn_HPC_LA31_N	G34	M29	34	V40	18
ADC	DATA2_P	ADC1/3_86	FMCn_HPC_LA28_P	H31	L29	34	V35	18
ADC	DATA2_N	ADC1/3_85	FMCn_HPC_LA28_N	H32	L30	34	V36	18
ADC	DATA3_P	ADC1/3_82	FMCn_HPC_LA29_P	G30	T29	34	W36	18
ADC	DATA3_N	ADC1/3_81	FMCn_HPC_LA29_N	G31	T30	34	W37	18
ADC	DATA4_P	ADC1/3_78	FMCn_HPC_LA24_P	H28	R30	34	U34	18
ADC	DATA4_N	ADC1/3_77	FMCn_HPC_LA24_N	H29	P31	34	T35	18
ADC	DATA5_P	ADC1/3_74	FMCn_HPC_LA25_P	G27	K29	34	R33	18
ADC	DATA5_N	ADC1/3_73	FMCn_HPC_LA25_N	G28	K30	34	R34	18
ADC	DATA6_P	ADC1/3_70	FMCn_HPC_LA26_P	D26	J30	34	N33	18
ADC	DATA6_N	ADC1/3_69	FMCn_HPC_LA26_N	D27	H30	34	N34	18
ADC	DATA7_P	ADC1/3_66	FMCn_HPC_LA21_P	H25	N28	34	P35	18
ADC	DATA7_N	ADC1/3_65	FMCn_HPC_LA21_N	H26	N29	34	P36	18
ADC	DATA8_P	ADC1/3_62	FMCn_HPC_LA22_P	G24	R28	34	W32	18
ADC	DATA8_N	ADC1/3_61	FMCn_HPC_LA22_N	G25	P28	34	W33	18
ADC	DATA9_P	ADC1/3_58	FMCn_HPC_LA23_P	D23	P30	34	R38	18
ADC	DATA9_N	ADC1/3_57	FMCn_HPC_LA23_N	D24	N31	34	R39	18
ADC	DATA10_P	ADC1/3_54	FMCn_HPC_LA19_P	H22	W30	34	U32	18
ADC	DATA10_N	ADC1/3_53	FMCn_HPC_LA19_N	H23	W31	34	U33	18
ADC	DATA11_P	ADC1/3_50	FMCn_HPC_LA20_P	G21	Y29	34	V33	18
ADC	DATA11_N	ADC1/3_49	FMCn_HPC_LA20_N	G22	Y30	34	V34	18
ADC	DRY_P	ADC1/3_46	FMCn_HPC_LA18_CC_P	C22	M32	34	U36	18
ADC	DRY_N	ADC1/3_45	FMCn_HPC_LA18_CC_N	C23	L32	34	T37	18

Figure C.1: Assignment table for the pins of the ADCs

ADC GPIO Pin Assignment

ADC0 / ADC2

					FPGA (FMC1)		FPGA (FMC2)	
LOC	**Signalname ADC**	**Pin ADC**	**Signalname FMC-HPC**	**Pin FMC**	**Pin**	**Bank**	**Pin**	**Bank**
ADC/GPIO	G0_P	ADC0/2_30	FMCn_HPC_HA11_P	J12	J37	35	AE34	16
ADC/GPIO	G0_N	ADC0/2_29	FMCn_HPC_HA11_N	J13	J38	35	AE35	16
ADC/GPIO	G1_P	ADC0/2_34	FMCn_HPC_HA10_P	K13	H38	35	AF31	16
ADC/GPIO	G1_N	ADC0/2_33	FMCn_HPC_HA10_N	K14	G38	35	AF32	16
ADC/GPIO	G2_P	ADC0/2_38	FMCn_HPC_HA14_P	J15	E37	35	AF35	16
ADC/GPIO	G2_N	ADC0/2_37	FMCn_HPC_HA14_N	J16	E38	35	AF36	16
ADC/GPIO	G3_P	ADC0/2_42	FMCn_HPC_HA17_CC_P	K16	C35	35	AC34	16
ADC/GPIO	G3_N	ADC0/2_41	FMCn_HPC_HA17_CC_N	K17	C36	35	AD35	16

ADC1 / ADC3

					FPGA (FMC1)		FPGA (FMC2)	
LOC	**Signalname ADC**	**Pin ADC**	**Signalname FMC-HPC**	**Pin FMC**	**Pin**	**Bank**	**Pin**	**Bank**
ADC/GPIO	G0_P	ADC1/3_30	FMCn_HPC_HA18_P	J18	F39	35	AB36	16
ADC/GPIO	G0_N	ADC1/3_29	FMCn_HPC_HA18_N	J19	E39	35	AB37	16
ADC/GPIO	G1_P	ADC1/3_34	FMCn_HPC_HA21_P	K19	D37	35	AA34	16
ADC/GPIO	G1_N	ADC1/3_33	FMCn_HPC_HA21_N	K20	D38	35	AA35	16
ADC/GPIO	G2_P	ADC1/3_38	FMCn_HPC_HA22_P	J21	F36	35	Y35	16
ADC/GPIO	G2_N	ADC1/3_37	FMCn_HPC_HA22_N	J22	F37	35	AA36	16
ADC/GPIO	G3_P	ADC1/3_42	FMCn_HPC_HA23_P	K22	A35	35	Y37	16
ADC/GPIO	G3_N	ADC1/3_41	FMCn_HPC_HA23_N	K23	A36	35	AA37	16

Amplification Board GPIO Pin Assignment

Board0 / Board2

					FPGA (FMC1)		FPGA (FMC2)	
LOC	**Signalname**	**Pin**	**Signalname FMC-HPC**	**Pin FMC**	**Pin**	**Bank**	**Pin**	**Bank**
AMP	A0_P	JP1_1	FMCn_HPC_HA04_P	F7	F34	35	AB29	16
AMP	A0_N	JP1_2	FMCn_HPC_HA04_N	F8	F35	35	AC29	16
AMP	A1_P	JP1_3	FMCn_HPC_HA05_P	E6	G32	35	Y32	16
AMP	A1_N	JP1_4	FMCn_HPC_HA05_N	E7	F32	35	Y33	16
AMP	A2_P	JP1_5	FMCn_HPC_HA03_P	J6	H33	35	AA29	16
AMP	A2_N	JP1_6	FMCn_HPC_HA03_N	J7	G33	35	AA30	16
AMP	A3_P	JP1_7	FMCn_HPC_HA02_P	K7	E33	35	AC30	16
AMP	A3_N	JP1_8	FMCn_HPC_HA02_N	K8	D33	35	AD30	16
AMP	A4_P	JP1_9	FMCn_HPC_HA07_P	J9	C38	35	AC31	16
AMP	A4_N	JP1_10	FMCn_HPC_HA07_N	J10	C39	35	AD31	16
AMP	A5_P	JP1_11	FMCn_HPC_HA06_P	K10	G36	35	AB31	16
AMP	A5_N	JP1_12	FMCn_HPC_HA06_N	K11	G37	35	AB32	16

Board1 / Board3

					FPGA (FMC1)		FPGA (FMC2)	
LOC	**Signalname**	**Pin**	**Signalname FMC-HPC**	**Pin FMC**	**Pin**	**Bank**	**Pin**	**Bank**
AMP	A0_P	JP2_1	FMCn_HPC_HA19_P	F19	B32	35	AC35	16
AMP	A0_N	JP2_2	FMCn_HPC_HA19_N	F20	B33	35	AC36	16
AMP	A1_P	JP2_3	FMCn_HPC_HA15_P	F16	C33	35	AE37	16
AMP	A1_N	JP2_4	FMCn_HPC_HA15_N	F17	C34	35	AF37	16
AMP	A2_P	JP2_5	FMCn_HPC_HA20_P	E18	B34	35	AD36	16
AMP	A2_N	JP2_6	FMCn_HPC_HA20_N	E19	A34	35	AD37	16
AMP	A3_P	JP2_7	FMCn_HPC_HA12_P	F13	B37	35	AF34	16
AMP	A3_N	JP2_8	FMCn_HPC_HA12_N	F14	B38	35	AG34	16
AMP	A4_P	JP2_9	FMCn_HPC_HA08_P	F10	J36	35	AA31	16
AMP	A4_N	JP2_10	FMCn_HPC_HA08_N	F11	H36	35	AA32	16
AMP	A5_P	JP2_11	FMCn_HPC_HA09_P	E9	E32	35	AE29	16
AMP	A5_N	JP2_12	FMCn_HPC_HA09_N	E10	D32	35	AE30	16

Figure C.2: Assignment table for the pins for the Attenuation and Amplification board and pins for the Digitization board, with the exception of the pins for the ADC

SMA GPIO Pin Assignment

					FPGA (FMC1)		FPGA (FMC2)	
LOC	**Signalname**	**Connector**	**Signalname FMC-HPC**	**Pin FMC**	**Pin**	**Bank**	**Pin**	**Bank**
FMC-ADC	SMACLK_0_P	X1	FMCn_HPC_LA00_CC_P	G6	K39	19	AD40	17
FMC-ADC	SMACLK_0_N	X2	FMCn_HPC_LA00_CC_N	G7	K40	19	AD41	17
FMC-ADC	SMACLK_1_P	X3	FMCn_HPC_LA17_CC_P	D20	L31	34	U37	18
FMC-ADC	SMACLK_1_N	X4	FMCn_HPC_LA17_CC_N	D21	K32	34	U38	18
FMC-ADC	SMACLK_2_P	X5	FMCn_HPC_HA00_CC_P	F4	E34	35	AB33	16
FMC-ADC	SMACLK_2_N	X6	FMCn_HPC_HA00_CC_N	F5	E35	35	AC33	16
FMC-ADC	SMACLK_3_P	X7	FMCn_HPC_HA01_CC_P	E2	D35	35	AD32	16
FMC-ADC	SMACLK_3_N	X8	FMCn_HPC_HA01_CC_N	E3	D36	35	AD33	16

Extension GPIO Pin Assignment

					FPGA (FMC1)		FPGA (FMC2)	
LOC	**Signalname**	**Connector**	**Signalname FMC-HPC**	**Pin FMC**	**Pin**	**Bank**	**Pin**	**Bank**
FMC-ADC	EXP0_0_P	JP3_1	FMCn_HPC_HB01_P	J24	H28	36	n/a	n/a
FMC-ADC	EXP0_0_P	JP3_3	FMCn_HPC_HB01_N	J25	H29	36	n/a	n/a
FMC-ADC	EXP0_1_P	JP3_4	FMCn_HPC_HB00_CC_P	K25	J25	36	n/a	n/a
FMC-ADC	EXP0_1_P	JP3_6	FMCn_HPC_HB00_CC_N	K26	J26	36	n/a	n/a
FMC-ADC	EXP0_2_P	JP3_7	FMCn_HPC_HB07_P	J27	G26	36	n/a	n/a
FMC-ADC	EXP0_2_N	JP3_9	FMCn_HPC_HB07_N	J28	G27	36	n/a	n/a
FMC-ADC	EXP0_3_P	JP3_10	FMCn_HPC_HB06_CC_P	K28	K23	36	n/a	n/a
FMC-ADC	EXP0_3_N	JP3_12	FMCn_HPC_HB06_CC_N	K29	J23	36	n/a	n/a
FMC-ADC	EXP0_4_P	JP3_13	FMCn_HPC_HB11_P	J30	K22	36	n/a	n/a
FMC-ADC	EXP0_4_N	JP3_15	FMCn_HPC_HB11_N	J31	J22	36	n/a	n/a
FMC-ADC	EXP0_5_P	JP3_16	FMCn_HPC_HB10_P	K31	M22	36	n/a	n/a
FMC-ADC	EXP0_5_N	JP3_18	FMCn_HPC_HB10_N	K32	L22	36	n/a	n/a
FMC-ADC	EXP0_6_P	JP3_19	FMCn_HPC_HB15_P	J33	M21	36	n/a	n/a
FMC-ADC	EXP0_6_N	JP3_21	FMCn_HPC_HB15_N	J34	L21	36	n/a	n/a
FMC-ADC	EXP0_7_P	JP3_22	FMCn_HPC_HB14_P	K34	J21	36	n/a	n/a
FMC-ADC	EXP0_7_N	JP3_24	FMCn_HPC_HB14_N	K35	H21	36	n/a	n/a
FMC-ADC	EXP0_8_P	JP3_25	FMCn_HPC_HB18_P	J36	G21	36	n/a	n/a
FMC-ADC	EXP0_8_N	JP3_27	FMCn_HPC_HB18_N	J37	G22	36	n/a	n/a
FMC-ADC	EXP0_9_P	JP3_28	FMCn_HPC_HB17_CC_P	K37	M24	36	n/a	n/a
FMC-ADC	EXP0_9_N	JP3_30	FMCn_HPC_HB17_CC_N	K38	L24	36	n/a	n/a
FMC-ADC	EXP1_0_P	JP4_1	FMCn_HPC_HB02_P	F22	K28	36	n/a	n/a
FMC-ADC	EXP1_0_P	JP4_3	FMCn_HPC_HB02_N	F23	J28	36	n/a	n/a
FMC-ADC	EXP1_1_P	JP4_4	FMCn_HPC_HB05_P	E24	K27	36	n/a	n/a
FMC-ADC	EXP1_1_P	JP4_6	FMCn_HPC_HB05_N	E25	J27	36	n/a	n/a
FMC-ADC	EXP1_2_P	JP4_7	FMCn_HPC_HB04_P	F25	H24	36	n/a	n/a
FMC-ADC	EXP1_2_N	JP4_9	FMCn_HPC_HB04_N	F26	G24	36	n/a	n/a
FMC-ADC	EXP1_3_P	JP4_10	FMCn_HPC_HB08_P	F28	H25	36	n/a	n/a
FMC-ADC	EXP1_3_N	JP4_12	FMCn_HPC_HB08_N	F29	H26	36	n/a	n/a
FMC-ADC	EXP1_4_P	JP4_13	FMCn_HPC_HB13_P	E30	P25	36	n/a	n/a
FMC-ADC	EXP1_4_N	JP4_15	FMCn_HPC_HB13_N	E31	P26	36	n/a	n/a
FMC-ADC	EXP1_5_P	JP4_16	FMCn_HPC_HB12_P	F31	K24	36	n/a	n/a
FMC-ADC	EXP1_5_N	JP4_18	FMCn_HPC_HB12_N	F32	K25	36	n/a	n/a
FMC-ADC	EXP1_6_P	JP4_19	FMCn_HPC_HB19_P	E33	L25	36	n/a	n/a
FMC-ADC	EXP1_6_N	JP4_21	FMCn_HPC_HB19_N	E34	L26	36	n/a	n/a
FMC-ADC	EXP1_7_P	JP4_22	FMCn_HPC_HB16_P	F34	N25	36	n/a	n/a
FMC-ADC	EXP1_7_N	JP4_24	FMCn_HPC_HB16_N	F35	N26	36	n/a	n/a
FMC-ADC	EXP1_8_P	JP4_25	FMCn_HPC_HB21_P	E36	P22	36	n/a	n/a
FMC-ADC	EXP1_8_N	JP4_27	FMCn_HPC_HB21_N	E37	P23	36	n/a	n/a
FMC-ADC	EXP1_9_P	JP4_28	FMCn_HPC_HB20_P	F37	P21	36	n/a	n/a
FMC-ADC	EXP1_9_N	JP4_30	FMCn_HPC_HB20_N	F38	N21	36	n/a	n/a

Figure C.3: Assignment table of additional pins for further expansions

APPENDIX D

Data transmission via serial UART interface

For the data transmission the same baud rate[1] is defined at transmitter and receiver, so that no clock signal is send with the data. To send a bit, the signal is pulled to *high* or *low* for a certain time and the bit can be read out using the previously defined build rate. Furthermore the specific sending pattern is also defined at transmitter and receiver, which is shown in figure D.1. While not sending data, the idle

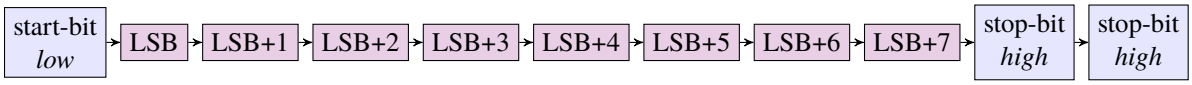

Figure D.1: Illustration of the sending pattern, in which the data is sent.

of the signal is *high*. Each sending of a 8 bit sequence starts with an start-bit, which is *low*, than the least significant bit (LSB) of the 8 bit sequence is sent, followed by the next bit and so on. The sending of the sequence stops with two stop-bits, which are both *high*. After the second stop-bit, the next 8 bit sequence can be sent, again starting with a start-bit. So that the negedge and posedge data are brought back into the correct sequence, they are sent alternately, as shown in figure D.2. A negedge sample point and a posedge sample point are taken one after the other and then sent together as 3 bytes. To indicate that a sending process has started, a total of 24 bit zeros are sent.

[1] Baud rate is the number of transmitted bits per second.

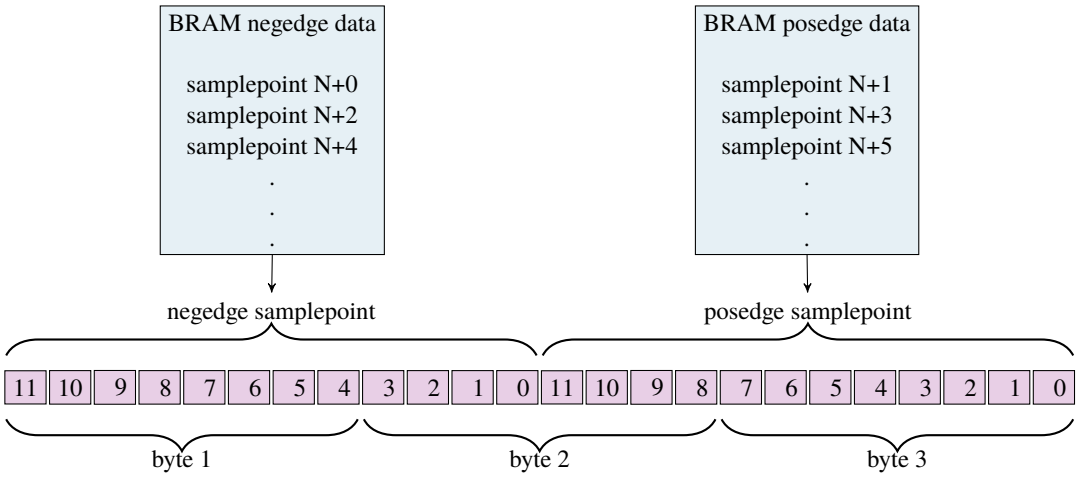

Figure D.2: In order to put the data in the correct order, a negedge samplepoint and a posedge samplepoint, each consisting of 12 bits, are always combined and sent in 3 bytes.

APPENDIX E

Evaluation of Digitization Board Version 1

The same measurement as described in section 4.4 was also performed for Digitization board version 1. The corresponding graph is shown in figure E.1. The same sinusodial equation

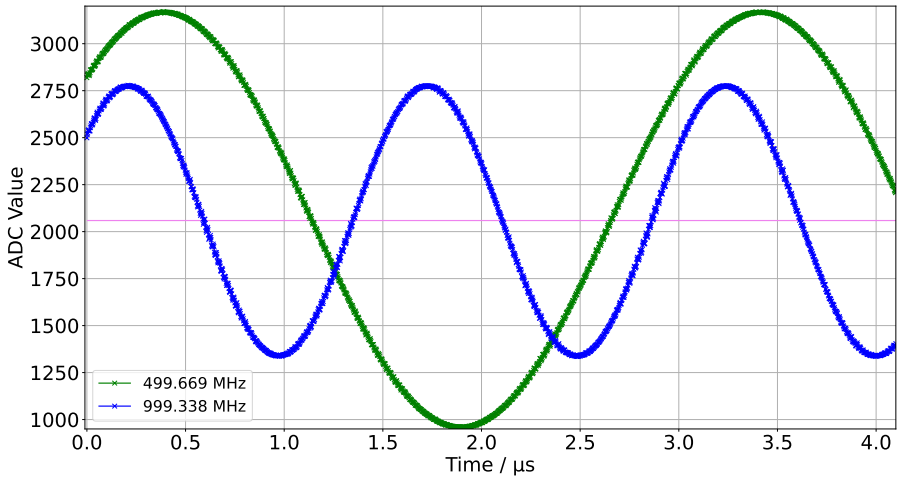

Figure E.1: Measurement with Digitization board version 1 of a sin of RMS-amplitude 600 mV maximal amplitude with frequency displayed in the plot. The zero line, displayed in table 4.1 is drawn in violet.

$$f(x) = a \cdot \sin(b \cdot x + c) + a_{\text{harm}} \cdot \sin\left(2 \cdot b \cdot x + c_{\text{harm}}\right) + d. \tag{E.1}$$

is fitted to the measured data points. The fitted parameters are show in table E.1.

Parameter	499.669 MHz	999.338 MHz
a / *ADC value*	1104.12 ± 0.04	717.64 ± 0.06
b / kHz	330.502 ± 0.003	661.035 ± 0.003
c	7.052200 ± 0.000008	6.9658 ± 0.0002
a_{harm}/ *ADC value*	6.30 ± 0.04	3.13 ± 0.06
c_{harm}	5.530 ± 0.007	7.990 ± 0.02
d	2058.63 ± 0.03	2051.23 ± 0.01

Table E.1: Fitted parameter of function E.1.

APPENDIX F

Measurement uncertainties evaluation for the filling pattern measurements

The buffering of the data of the test measurements of the filling structure is done in 8 times 2 individual block rams in the FPGA (8 BRAMs for the data that are read out on the posedge and 8 for that of the negedge (see section 4.3.2). The first element of the BRAM is not updated due to a bug in the implementation and is therefore not correct, resulting in a larger errorbar, which is shown in figure F.1. The plot shows the uncorrected measurement data from measurement 5.2. The larger error bars

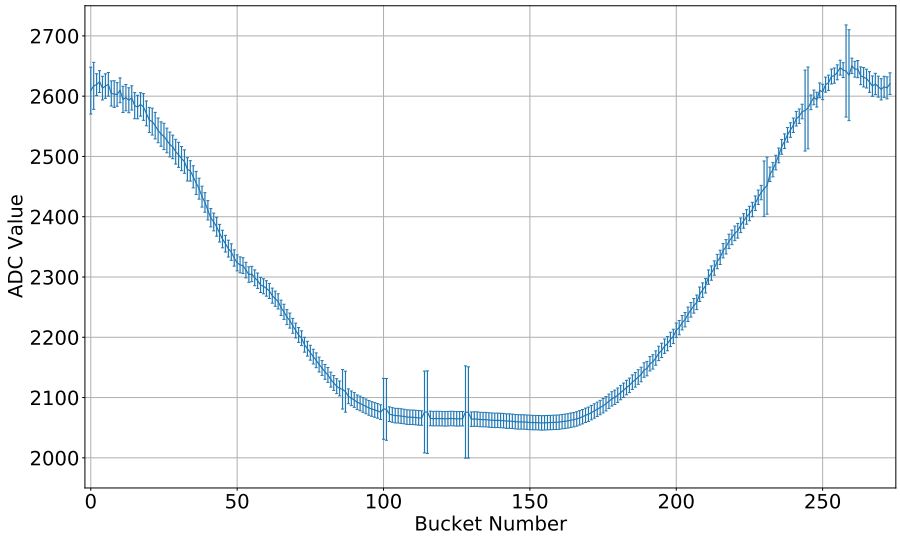

Figure F.1: The raw data of the filling pattern of the inhomogeneous filling is shown. It can be seen, that the errorbars for bunch 0 and 1, 86 and 87, 100 and 101, 113 and 114, 127 and 128, 230 and 231, 244 and 245, 258 and 259 are larger than the other errorbars.

of the measured values for the bunches 0 and 1, 86 and 87, 100 and 101, 113 and 114, 127 and 128, 230 and 231, 244 and 245, 258 and 259 can each be assigned to the first value of a block ram. These

incorrectly recorded data are not taken into account for the correct evaluation of the data.

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